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Based on the understanding and the conclusions from the simulation and measurement results, concrete EMI optimization concepts for an inherently low-interference power module are developed and realized. The EMI performance as well as the feasibility of the sample modules are compared and evaluated under different criteria from the power module manufacturer's point of view. Besides, the dynamic and short-circuit performances of the sample modules, regarding to the current distribution on the semiconductor chips, are characterized.
A novel test procedure is introduced in this work, by which it is possible to estimate the conducted EMI performance of power modules without building the whole test setup like in a conventional EMI measurement. This characterization can subsequently be used in the phase of converter development to select a suitable device and evaluate the expected effort to comply with EMI standards.

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Dissertation

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- Prof. Dr. rer. nat. habil. Jürgen Nitsch
- Prof. Dr.-Ing. habil. Zbigniew Antoni Styczynski

alle: Otto-von-Guericke-Universität Magdeburg
Postfach 4120, 39016 Magdeburg

V. i. S. d. P.:

Dr.-Ing. Yu Liu
Otto-von-Guericke-Universität Magdeburg, Postfach 4120, 39016 Magdeburg

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Warstein, April 2021

Yu Liu

Abstract

This work serves as a contribution to improve the EMI performance of electrical drive systems in vehicles; the focus is on the power semiconductor module for automotive application.

For a better and deeper understanding of the conducted EMI source, the conducted EMI mechanisms and effects in the drive system are investigated through simulations as well as measurements with special consideration of power modules: The influence of the diode recovery effects on the EMI performance is quantitatively analyzed with different load currents, as well as with different types of diodes, e.g. SiC Schottky barrier diode. Through the simulation, the influence coming from the power module to the system is clarified; the importance of different factors inside and outside of the power module regarding EMI performance are therefore evaluated. To validate the simulation results, the setup and test bench for a conventional EMI measurement for the typical automotive application are presented. Through the measurement results it is proven that the simulation models are usable under certain boundary conditions for future power module designs with regard to the EMI prediction.

Based on the understanding and the conclusions from the simulation and measurement results, concrete EMI optimization concepts for an inherently low-interference power module are developed and realized. The EMI performance as well as the feasibility of the sample modules are compared and evaluated under different criteria from the power module manufacturer's point of view. Besides, the dynamic and short-circuit performances of the sample modules, regarding to the current distribution on the semiconductor chips, are characterized.

A novel test procedure is introduced in this work, by which it is possible to estimate the conducted EMI performance of power modules without building the whole test setup like in a conventional EMI measurement. This characterization can subsequently be used in the phase of converter development to select a suitable device and evaluate the expected effort to comply with EMI standards.

Keywords

EMI, Power module, Automotive application, FFT, Diode reverse recovery, SiC diode, dv/dt, Time-domain simulation, Passive measurement, HF-modeling, Resonance frequency, DCB layout, Parasitic capacitance, Snubber, X-capacitor, Y-capacitor

Kurzfassung

Diese Arbeit dient als Beitrag zur Verbesserung des EMV-Verhaltens elektrischer Antriebssysteme in Fahrzeugen, wobei der Fokus auf dem Leistungshalbleitermodul für die Automobilanwendung liegt.

Für ein besseres und tieferes Verständnis der Quelle von leitungsgebundenen Störungen werden die EMV-Mechanismen und -Effekte im Zusammenhang mit dem Leistungsmodul im Antriebssystem durch Simulationen und Messungen untersucht. Der Einfluss der Diode Reverse Recovery Effekte auf das EMV-Verhalten wird quantitativ mit verschiedenen Lastströmen sowie mit verschiedenen Diodentypen, wie z.B. SiC-Schottky-Dioden, analysiert. Durch Simulationen wird der Einfluss des Leistungsmoduls auf das System untersucht; auf dieser Basis wird die Bedeutung verschiedener Faktoren innerhalb und außerhalb des Leistungsmoduls für das EMV-Verhalten bewertet. Zur Validierung der Simulationsergebnisse wird der Messaufbau für eine konventionelle EMV-Messung für die Automobilanwendung vorgestellt. Die Messergebnisse belegen, dass die Simulationsmodelle unter bestimmten Randbedingungen für zukünftige Leistungsmodulkonstruktionen zur EMV-Vorhersage verwendbar sind.

Basierend auf dem Verständnis, wie es aus den Simulationen und Messergebnissen hergeleitet wurde, werden konkrete Optimierungskonzepte für ein inhärent störungsarmes Leistungsmodul entwickelt und realisiert. Dessen EMV-Verhalten sowie der Aufwand des Musterbaus aus Sicht des Leistungsmodulherstellers werden anhand verschiedenen Kriterien verglichen und bewertet. Außerdem wird das dynamische und Kurzschlussverhalten der Prototypen einschließlich der Stromverteilung zwischen den Halbleiterchips charakterisiert.

In dieser Arbeit wird ein neuartiges Testverfahren vorgestellt, mit dem es möglich ist, das leitungsgebundene EMV-Verhalten von Leistungsmodulen abzuschätzen, ohne den gesamten Testaufbau wie bei einer konventionellen EMV-Messung zu erstellen. Diese Charakterisierung kann anschließend in der Phase der Inverterentwicklung verwendet werden, um ein geeignetes Modul auszuwählen und den erwarteten Aufwand zur Einhaltung der EMV Standards zu bewerten.

List of publications

i) Y. LIU, S. CORDES, T. GEINZER, J. THIELE, M. THOBEN and A. LINDEMANN: *Comparison of EMI behavior in inverter and buck-converter operation of power modules by considering the diode reverse recovery effects*. CIPS 2016, 9th International Conference on Integrated Power Electronics Systems, Nürnberg, 2016.

ii) Y. LIU, S. KOCHETOV, T. SMAZINKA and A. LINDEMANN: *Characterizing the Conducted EMI Performance of a Power Module through Passive Measurement*. PCIM Europe 2017, International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, Nürnberg, 2017.

iii) Y. LIU, T. GEINZER, S. CORDES and J. THIELE: *Inhärent Störungsarme Leistungselektronik - InSeL : Teilvorhaben: Infineon Technologies AG : EMV-gerechtes Design von Leistungselektronikmodulen für Automotive-Anwendungen : Schlussbericht InSeL : Berichtszeitraum: 01.01.2014 bis 31.12.2016*. TIB/BMBF-Bibliothek, Infineon Technologies AG, München, 2017.

Contents

List of Acronyms

AC	Auxiliary Collector / Alternating Current
AE	Auxiliary Emitter
AMB	Active Metal Brazed
CENELEC	European Committee for Electrotechnical Standardization
CISPR	International Special Committee on Radio Interference
CM	Common Mode
DC	Direct Current
DCB	Direct Copper Bonded
DM	Differential Mode
DRR	Diode Reverse Recovery
EMI	Electromagnetic Interference
ESL	Equivalent Series Inductivity
ESR	Equivalent Series Resistance
FCC	Federal Communications Commission
FFT	Fast Fourier Transform
HF	High Frequency (3 - 30 MHz)
HS	High Side
HV	High Voltage in automotive application (less than 1 kV, normally 400 V)
IEC	International Electrotechnical Commission
ISO	International Organization for Standardization

LF	Low Frequency (30 - 300 kHz)
LISN	Line Impedance Stabilization Network
LS	Low Side
LV	Low Voltage
MF	Medium Frequency (300 - 3000 kHz)
PDS	Power Drive System
PWM	Pulse Width Modulation
RBSOA	Reverse Bias Safe Operating Area
RMS	Root Mean Square
SCM	Similar Common Mode
VHF	Very High Frequency (30 - 300 MHz)
VNA	Vector Network Analyzer

List of Symbols

A	Amplitude of the trapezoidal pulse
a	Distance between two wires
$C_{+,-}$	Parasitic capacitances of the positive and negative power module potential
$C_{1,2}$	Capacitors in LISN
C_{CE}	Collector-emitter capacitance of the IGBT
C_{Diode}	Diode capacitance
C_{GC}	Gate-collector capacitance of the IGBT
C_{GE}	Gate-emitter capacitance of the IGBT
C_{HS_chip}	Chip capacitance of the half-bridge high-side
C_K	Coupling capacitance
C_{LS_chip}	Chip capacitance of the half-bridge low-side
C_{out}	Output capacitance of the power module's AC knot
C_S	Cable shields capacitance
$C_{W,g}$	E-machine windings capacitance
E_{off}	Switching loss by IGBT turn-off
E_{on}	Switching loss by IGBT turn-on
E_{sum}	Sum of turn-on loss and turn-off loss
F	Fall time of the trapezoidal pules
F'	Normalized Fall time of the trapezoidal pules
$f_{k1,2,3}$	Knee frequencies of the spectrum
f_{switch}	Switching frequency

I_C	Current flowing in IGBT
I_{CES}	Collector-emitter cut-off current
$I_{CM1,2}$	Leakage currents
I_{CN}	Implemented collector current of the power module
$I_{DC,buck}$	Current in the buck-converter operation mode
I_F	Current flowing in diode
I_{Load}	Load current
I_{rec}	Reverse recovery current of the diode
$I_{RMS,inv}$	RMS current in the inverter operation mode
I_{RMS_Load}	RMS value of the load current
k	Multiples of the fundamental frequency
l	Length of the wire
$L_{+,-}$	Stray inductances of the positive and negative power module potential
L_1	Inductors in LISN
$L_{input,output}$	Stray inductances of the power module pins
L_p	Inductance per length
L_s	Stray inductance of cable or bond wire
M	Average duration of the trapezoidal pulse
m	Modulation degree of the PWM
M'	Normalized average duration of the trapezoidal pulse
R	Rise time of the trapezoidal pulse
R'	Normalized rise time of the trapezoidal pulse
r_0	Radius of the wire
$R_{1,2}$	Resistors in LISN
T	Period of the trapezoidal pules
T_{f0}	Fundamental period of the sinusoidal current

t_{fall}	Fall time of the switching edge
t_p	Duration of the plateau in trapezoidal pules
T_{pulse}	Defined time interval
t_{rise}	Rise time of the switching edge
U_{AC}	Output voltage by each AC knot of the half-bridge
$U_{DC+,-}$	DC-link voltage
V_{Bat}	Battery potential of the EV
V_{CE}	Collector-emitter voltage of the IGBT
V_F	Forward voltage drop on the diode
V_R	Reverse voltage drop on the diode
V_{GE}	Gate-Emitter voltage of the IGBT
V_{GEth}	Threshold voltage of the IGBT
V_{ind}	Induced voltage
Y	Admittance curve from the passive measurement
Z_{Ground}	Impedance defined connecting the heat-sink and the electric circuit of the power module
ε_r	Relative permittivity
μ	Permeability

1. Introduction

Power electronics is a key element for the low-loss conversion of electrical energy. In an electrical drive system, the motor speed can be controlled by using an inverter. In an energy conversion system, e.g., the voltage level can be adjusted by using a DC/DC converter. However, in a vehicles' drive system, to integrate the inverter, the DC/DC converter and the charging equipment etc. into extremely limited space, it is very difficult to comply with the EMI limits and keep the EMI immunity, since during the signal transmission, the internal devices in the vehicle can interfere with each other. In order to meet all the requirements for future use in electrified drives, from the economic and space view, an EMC-optimized design of the submodules in the system, the use of targeted shielding / filtering measures as well as optimal PCB layouts, are absolutely necessary [5][80].

The main motivation of this dissertation is to research and optimize the main source of the EMI: -the power module. In this work, scientific concepts, simulation and measurement methods for designing the novel, low-interference power modules are developed and implemented. Some demonstrators are realized, characterized and then evaluated with regard to their EMI potential as well as other criteria. A newly developed measurement method is also intended to enable the power module manufacturer to pre-evaluate the products' EMI behavior without obtaining the concrete system information from the vehicle OEMs.

Generally, this dissertation is organized as follows:

Chapter 2 gives the state of the art of the conducted EMI and its main source, the power semiconductor module. The origin, spreading and coupling mechanisms of the conducted EMI are explained; the relevant standards that are currently used in industrial and automotive applications are summarized and compared. Besides, the relevant basic knowledge about the dynamic performance of the semiconductors within the power module is indroduced; the recommended manner of the dynamic characterization of the power modules is also presented.

Chapter 3 investigates some effects regarding the source of the conducted EMI, i.e., the switching edges of the semiconductor with large $\mathrm{dv/dt}$. The content mainly includes: the spectrum analysis of the unideal switching edge which contains a plateau, the discussion of the inconstant $\mathrm{dv/dt}$ of the switching edges that are caused by the DRR effect as well as the variable load current, the expectation and validation of the switching edges' $\mathrm{dv/dt}$ that are produced by a SiC diode without DRR effect. According to these investigations, some conclusions are drawn regarding the EMI performance of the power converter's different operation modes.

In chapter 4, based on the understanding of the effects of the EMI source, the discussion is extended into the level of the drive system in the automotive application. For the later improvement of the power module's EMI performance, the simplified time-domain simulation models on system-level are built up. Through the simulation, the influences coming from the power module to the system can be better clarified; the importance of different factors inside / outside of the power module can be therefore evaluated. To validate the simulation results, the

setup and test bench of the conventional EMI measurement for a typical automotive application are presented. The measurement approaches used in this dissertation are explained and discussed.

From the power module manufacturer's point of view, performing a basic EMI qualification of its products independent on the system makes sense. In chapter 5, based on some existing research results, the usage of a new test procedure makes it possible to estimate the conducted EMI performance of the power module without building the whole test setup like in a conventional EMI measurement. This characterization can subsequently be used in the phase of converter development to select a suitable device and evaluate the expected effort to comply with EMI standards.

In chapter 6, as the main motivation of this dissertation, the research for the EMI optimization of the power module is described. Based on the researched power modules for industrial applications by Domurat-Linde and Domes, the EMI optimization concepts are extended to cover the power modules for automotive application. Using the measurement and simulation results in chapter 3 and 4, further ideas and solutions for the inherent low-interference power module are developed and realized in Infineon®'s HybridPACK™ 2 module package for EV application. The EMI performance as well as the feasibility of the sample modules are compared and evaluated under different criteria from the power module manufacturer's point of view. Besides, the dynamic and short-circuit performances of the sample modules are characterized, in order to specially investigate the new current distribution on the semiconductor chips due to the changed DCB layout structure and the switching losses because of the insertion of the external capacitors.

Chapter 7 closes this dissertation with some conclusions and future work.

From the flow chart's point of view, the methodology and procedure of this dissertation are mainly presented by 5 parts as shown in Fig. 1-1:

- Investigations about the EMI source
  In this part some interesting effects regarding the conducted EMI source are investigated (referring chapter 3).
- Modeling / measuring the transfer-admittance at component level
  In this part the system components in the drive system are modeled or measured. Since the conducted EMI are transferred by them, the natural frequency of these components can magnify the EMI in some frequency ranges (referring chapter 4 and 5).
- Time-domain simulation on system level
  For this part, the EMI source and its transfer paths (admittance) are combined to establish a simplified drive system in the simulation, so that the influences coming from the power module to the system can be better clarified; the importance of different factors inside / outside of the power module can therefore be evaluated. This lays the foundation for how the EMI elements shall be considered in the optimization of power modules for the next part.
- EMI optimization with special consideration of power module
  Based on the understanding of the effects as well as the gained knowledge from the above parts, the conducted EMI optimization on the power module can finally be implemented in this part.
- Verification of the results by conventional EMI measurements

The research results in all above parts are respectively verified through the conventional EMI measurements.

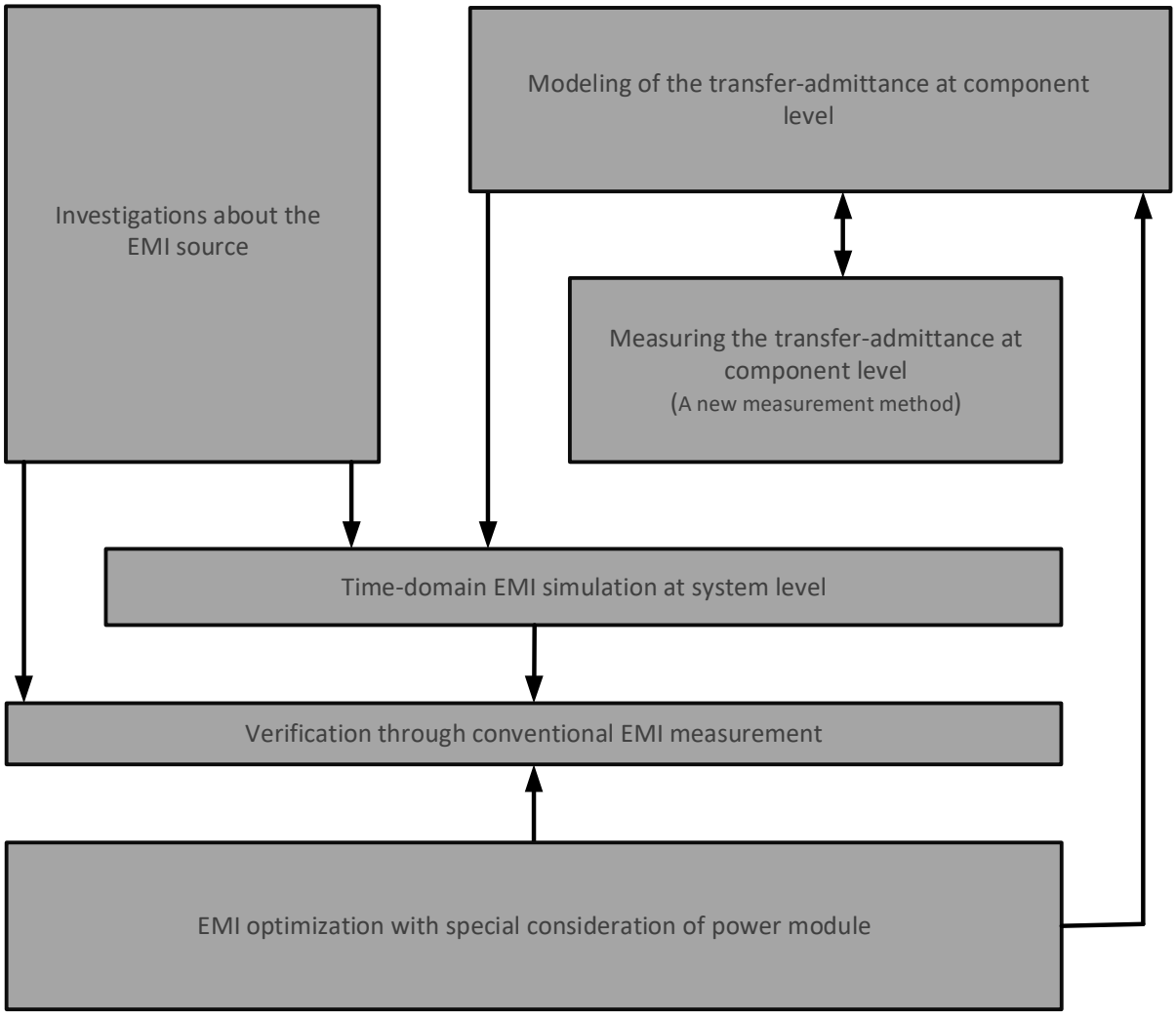


Fig. 1-1: Flow chart of the dissertation

2. State of the art

2.1. Conducted electromagnetic interference

According to the Official Journal of the European Union, the EMC is defined as "the ability of equipment to function satisfactorily in its electromagnetic environment without introducing intolerable electromagnetic disturbances to other equipment in that environment" [75]. In other words, the equipment must not cause interference to other equipment in its surroundings nor to itself and must not be susceptible to emissions from other systems. Consequently, EMC is concerned with the generation, transmission and reception of electromagnetic disturbances [76]. In general, the electromagnetic interference energy, commonly called the EMI, is generated by an interference source, and then transmitted through a coupling path into a receiver.

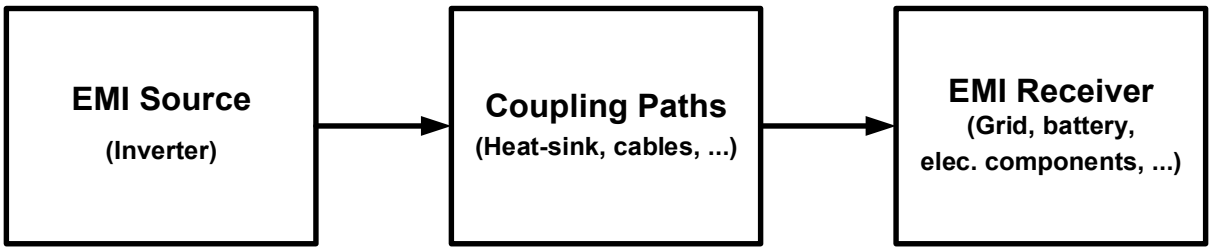


Fig. 2-1: Basical decomposition of the EMI issue

The simplified diagram in Fig. 2-1 illustrates this described situation: The power electronics are a source of electromagnetic interference. Because of the fast switching behavior with high voltages and currents, on the one hand, the electromagnetic fields can propagate into the environment; on the other hand, high-frequency currents can be conducted through the wires within the system. Through the coupling paths, the electromagnetic interference can transmit from the source to the receiver. In the case of the power electronics, the grid for power supply in industrial applications, as well as the HV-battery or another electrical component in automotive applications, can be considered as the receiver of the interference. The optimization of the EMI performance can thereby be concluded in three aspects [76]:

- Suppressing the emission at its source,
- Making the coupling path as inefficient as possible,
- Making the reveiver less susceptible to the emission.

In this dissertation, the research is focused on the conducted EMI and its reduction; the radiated EMI is not to be discussed, since nowadays in the automotive and industrial applications, the radiated emissions can usually be defended by using shielding measures. In 2.1.1, the inverter as EMI source of the system will be introduced; in 2.1.2, the coupling paths as well as the interference spreading mechanisms are explained. In 2.1.3, from the EMI

receiver side of view, relevant standards regarding the EMI requirements in automotive and industrial applications are summarized and compared with each other.

2.1.1. Origin of conducted EMI

Nowadays, electrical motor drives are widely used in electromechanical energy conversion systems. Working as one of the key components in the drive system, the modern power electronic converters can generate the AC voltage with targeted frequency and amplitude from a DC or AC voltage supply. Depending on the specific application, different types of power converters can be used. One of the most commonly used types in automotive application, consisting of battery, DC-link and inverter, is shown schematically in Fig. 2-2.

The HV (High Voltage) battery working as input-part of the power converter system can usually be considered as a DC voltage supply. The DC voltage is then smoothed by the DC-link capacitor. The inverter working as output-part of the power converter system consists of three half-bridges, each composed of two IGBTs in high and low side with associated free-wheeling diode. The inverter converts the DC-link voltage into an AC voltage of the targeted frequency, amplitude and phase position, which is required for driving the electrical motor of the load side. For this purpose, the IGBTs are switched on and off via the drive board with the PWM (Pulse Width Modulation) signals, the output voltage U_{AC} by each AC knot of the inverter switches between the values $+U_{DC}/2$ and $-U_{DC}/2$ to form a series of pulses. Through the chronological changing of the pulse widths, the mean value of U_{AC} over a defined time interval T_{pulse} results in different output voltages whose values lie in between $+U_{DC}/2$ and $-U_{DC}/2$ (see Fig. 2-3 top). Considering that this variable output voltage drops on the motor from the load side, the charging and discharging of the inductive coil will take place alternately along with the IGBT switching. In this way, the sinusoidal load current with the fundimental period of T_{f0} (see Fig. 2-3 bottom) can be produced in each phase of the inverter.

Within a half-bridge of the inverter, the two IGBTs must not be switched on at the same time. Either the high side or the low side IGBT is switched on by the PWM signal. The current commutation between the IGBT's ON and OFF states always takes place within the half-bridge, combined with the free-wheeling diode of the opposite respectively. Since the high side and the low side switch from different half-bridges perform analogously with each other, it is acceptable to simplify the inverter operation as a buck-converter operation in order to focus on the study of the switching performances [10][11][74]. The feasibility as well as disadvantages of such simplification from the EMI point of view will be further discussed in chapter 3.2.

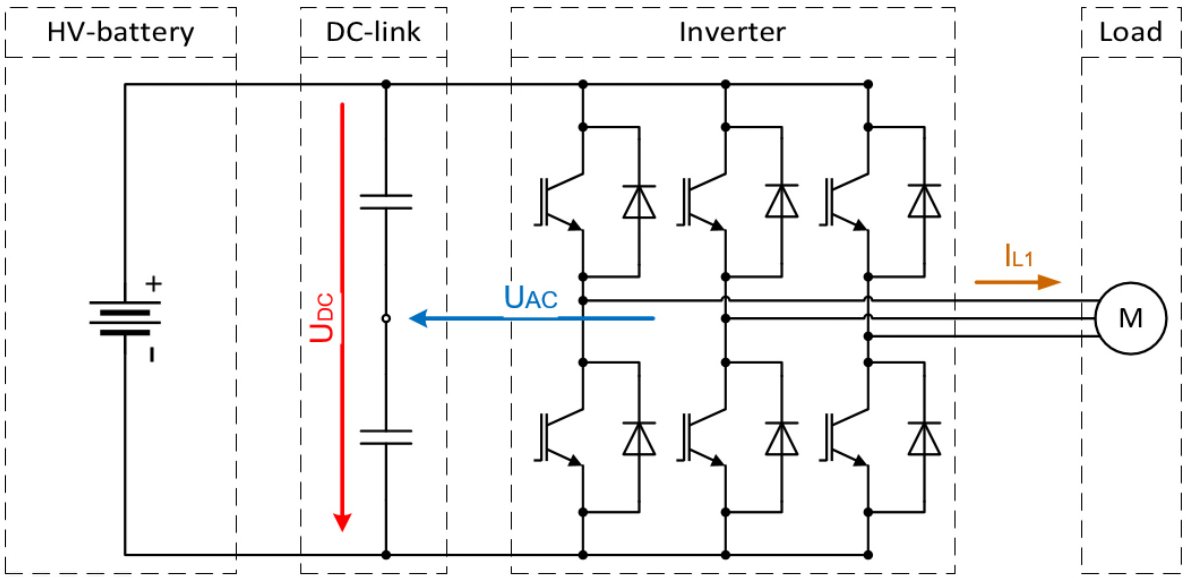


Fig. 2-2: Schematic diagram of a three-phase power converter consisting with HV-battery, DC-link and inverter

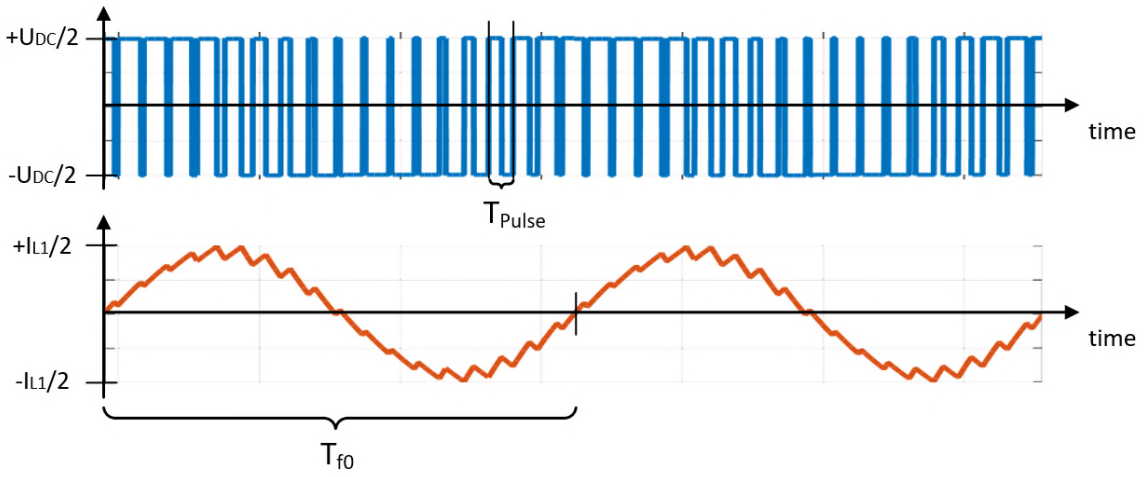


Fig. 2-3: Pulse width modulated signals: output voltage U_{AC} (top) and load current (bottom) from one phase of the inverter

Since the inverter is based on PWM techniques with switches characterized by very small switching times, the modulated output voltage signal in the HV drive system for the automotive application (less than 1 kV, normally 400 V) is pulse-shaped. The generated high voltage slew rate dv/dt and high current slew rate di/dt during the switching processes have been established as the main source of EMI in electrical applications [1][2][5][9][11][17][48][50][51].

For a better understanding of the EMI source, the pulse that is generated by the inverter can be approached by a trapezoidal curve in time-domain; its spectrum can be calculated analytically for the approximation. This result can be used as interference voltage source in a frequency-domain circuit simulation [1][5][53]. For example, to build up an interference source of the simulation model in [1], the output voltage of the AC knot during the IGBT switching has been measured, then approximated by a trapezoidal pulse overlaid with an oscillation of 33 MHz. After that it has been translated into a spectrum of 3 MHz to 300 MHz and used in the frequency-domain model which consists of a voltage source and other passive RLC components. The advantage of the analytical calculation of the spectrum is that the equation

can reveal the relationships between the parameters of the approached pulse in time-domain and the resulting spectrum in frequency-domain. It is thereby possible to find out how the spectrum is generated and which parts of the time-domain signal make a decisive contribution. Generally, the pulse in trapezoidal shape with defined parameters: a rise time R, a fall time F, the pulse's amplitude A and the average duration M (Fig. 2-4 left), is used as a typical object for the analytical calculation [1][2][5][51]. The average duration M means the time during which the signal $\mathrm{s(t)}$ is larger than half of its amplitude. For the calculation the parameters are normalized and marked with an apostrophe: $\mathrm{t'} = \mathrm{t/T}$, $\mathrm{M'} = \mathrm{M/T}$, $\mathrm{R'} = \mathrm{R/T}$ and $\mathrm{F'} = \mathrm{F/T}$. The total trapezoidal pulse can be described by three functions defined in sections [1]:

$$\begin{aligned} s_1(\mathrm{t'}) &= \frac{\mathrm{A}}{\mathrm{R'}} t' && ;0 \le t' < t_1' && ;\ t_1' = R' \\ s_2(\mathrm{t'}) &= \mathrm{A} && ;\ t_1' \le t' < t_2' && ;\ t_2' = \tfrac{R'}{2} + M' - \tfrac{F'}{2} \\ s_3(\mathrm{t'}) &= \tfrac{\mathrm{A}}{\mathrm{F'}}\left(M' + \tfrac{\mathrm{R'}}{2} + \tfrac{\mathrm{F'}}{2} - \mathrm{t'}\right) && ;\ t_2' \le t' \le t_3' && ;\ t_3' = \tfrac{R'}{2} + M' + \tfrac{F'}{2} \end{aligned} \qquad \textbf{(2-1)}$$

By considering that the pulse will repeat uniformly, the continuous Fourier transformation can be carried out, when the period T of the time-domain trapezoidal signal $\mathrm{s(t)}$ is taken into account:

$$\begin{aligned} \frac{\mathrm{S}(\omega')}{2} = &\int_0^{R'} \frac{A}{R'} \cdot t' \cdot \mathrm{e}^{-\mathrm{j}\omega' \cdot \mathrm{t}'} dt' + \int_{R'}^{\frac{R'}{2}+M'-\frac{F'}{2}} A \cdot \mathrm{e}^{-\mathrm{j}\omega' \cdot \mathrm{t}'} dt' \\ &+ \int_{\frac{R'}{2}+M'-\frac{F'}{2}}^{\frac{R'}{2}+M'+\frac{F'}{2}} \left(\frac{\mathrm{A}}{\mathrm{F'}}\left(M' + \frac{\mathrm{R'}}{2} + \frac{\mathrm{F'}}{2} - \mathrm{t'}\right)\right) \cdot \mathrm{e}^{-\mathrm{j}\omega' \cdot \mathrm{t}'} dt' \end{aligned} \qquad \textbf{(2-2)}$$

The equation (2-3) shows the solution of the integral calculus for the signal $\mathrm{s(t)}$ in Fig. 2-4 left. The detailed explanation of the mathematic calculation can be found in [1]. As an alternative solution, the purpose can also be fulfilled by programing in MATLAB, using its discrete FFT (Fast Fourier Transformation) and other relevant functions.

$$\mathrm{S(k)} = \frac{\mathrm{A}}{\pi \mathrm{k}}\left[\mathrm{si}(\pi \mathrm{kR'}) \cdot \mathrm{e}^{\mathrm{j}\pi \mathrm{kM'}} - \mathrm{si}(\pi \mathrm{kF'}) \cdot \mathrm{e}^{-\mathrm{j}\pi \mathrm{kM'}}\right] \quad ;\mathrm{k} = \mathrm{fT} \qquad \textbf{(2-3)}$$

According to the Fourier transformation result from equation (2-3), it is possible to determine the approximation line for the maximum limits of the spectrum. The approximation is nothing more than calculating the envelope curve of the spectrum. According to [5], the approximation line can be divided into different parts and then described by different functions. The dividing points in frequency range are called "knee points". As shown in Fig. 2-4, there are usually at least two knee points $\mathrm{f_{k1}}$ and $\mathrm{f_{k2}}$ visible. The characteristics of the approximation line have been summarized by [5] like this: (translated from German) "Before the frequency reaches the knee point $\mathrm{f_{k1}}$, the spectrum's amplitude is enveloped by its fundamental's amplitude. The value of $\mathrm{f_{k1}}$ is usually larger than the switching frequency $1/\mathrm{T}$ and reaches its minimum $1/\mathrm{T}$ when the average duration $\mathrm{M'}$ is equal to 0.5. For shorter or longer $\mathrm{M'}$, $\mathrm{f_{k1}}$ reaches values greater than $1/\mathrm{T}$. Above of $\mathrm{f_{k1}}$, the amplitude of the spectrum decreases. In logarithmic terms this means a drop of 20 dB per frequency decade. From the second knee point $\mathrm{f_{k2}}$, the amplitude is determined by the smoother one of the two switching edges (rise and fall). If the

rise-time R and fall-time F are the same, there will be amplitude dropping of 40 dB per decade here. Above f_{k2}, the switching edges significantly determine the magnitude of the amplitude, with the steeper edge causing the higher spectrum."

Such envelope approximation includes also the situations like for those pulses by $R' = F' = 0$ (idealized rectangular pulses) or by $M' = \frac{R'+F'}{2}$ (unbalanced triangular pulses). The corresponding spectrums of these pulses are schematically presented in Fig. 2-5.

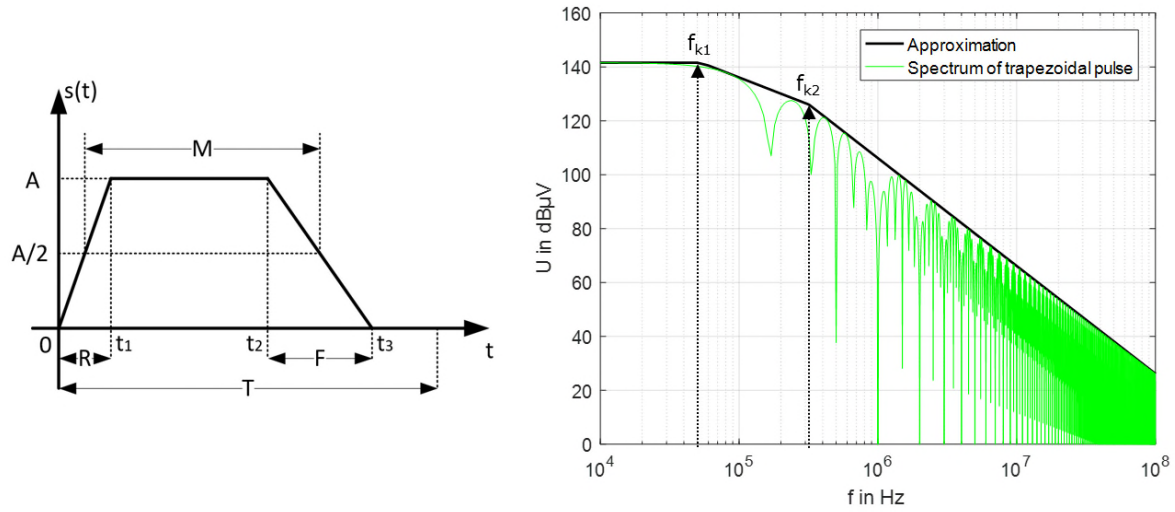


Fig. 2-4: Definition of the trapezoidal pulse in time-domain (left) and its spectrum in frequency-domain in two representations (right)

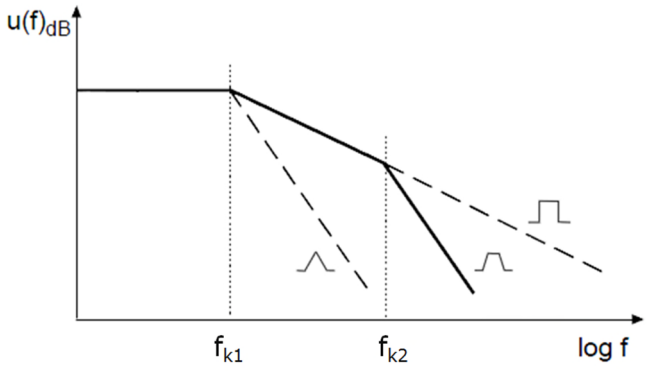


Fig. 2-5: Amplitude forms for trapezoid, rectangle and triangle pulses

2.1.2. Spreading and coupling mechanisms of conducted EMI

As common sense of the contemporary investigations regarding the EMI, the conducted interferences are usually divided into Differential-Mode (DM) and Common-Mode (CM) noises depending on their origins. The interference modes can convert from one to the other in the power electronics circuits because of unbalance of the system components [1][57][70].

The basic concept of the conducted EMI in DM and CM modes for a single phase are illustrated in Fig. 2-6. By the DM interference, the interference current usually flows within the HV system to build up a closed loop. That means the EMI current transfers along with the load current from one phase to another phase of the system, disturbing the wanted signals by the high frequency noises. Thus, the DM interference is referred to as a symmetrical noise.

By the CM interference, the EMI current transfers though the two (or more) wires of the HV system in the same direction, then returns to its source to close the loop by flowing across the GND. This interference can therefore be measured with the GND as reference. The CM interference is usually generated by potential fluctuation against ground due to the charge and discharge of the parasitic capacitances existing between the HV system and the GND. The CM interference is referred to as asymmetrical noise.

In the electrical applications, both types of interferences are produced simultaneously and are inseparable. According to [68][69][70] and [79], the DM and CM interferences can interact with each other, generating a sort of mixed-mode (MM) interference phenomenon.

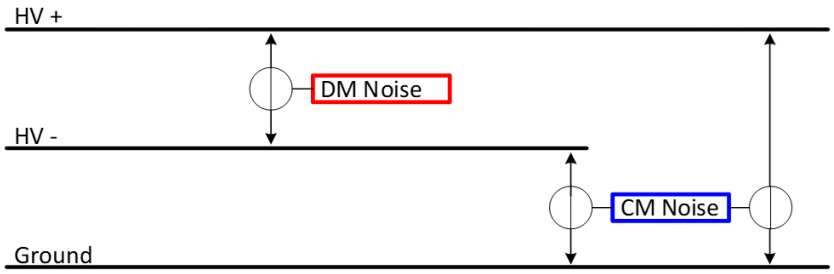


Fig. 2-6: Basic concept of conducted EMI in differential- and common-mode

The switching speed of current silicon (Si) and new silicon carbide (SiC) or gallium nitride (GaN) devices is becoming even higher, enabling the development of even smaller and more efficient inverters. However, due to the faster switching edges, high leakage currents also flow via the coupling capacitance C_K (see Fig. 2-7) from the HV half-bridge to the inverter heat-sink, via cable shields capacitance C_S or the winding capacitance C_W in the electrical machine, which leads to high common-mode EMI.

The research regarding the modeling of the motor cables (L_S and C_S) can be referenced by literature such as [43][44][45]. For example, to analyze and reduce the EMI generated by the inverter used with a long motor cable, it is necessary to build a satisfactory model of the cable, which should take into account the skin effect [42][46][47] and the proximity effect as well as the dielectric losses. In [43], a finite-element method is used to calculate most of the electrical parameter values of the energy cable model. The proposed unshielded and shielded models were validated in both the frequency and time domains. From the application point of view, while frequency-domain models inherently rely on matrix representations, time-domain models require to build equivalent circuits in the form of numerous cascaded cells to account for propagation phenomena in the cables. Thus, the time-domain simulation is well suited for power converters because semiconductor devices operate in large signal commutation mode, with a strongly nonlinear behavior. However, the frequency domain is best suited for high-frequency modeling, which is required for EMC simulations [44]. The frequency domain model proposed by Marlier, Videt and Idir allows a significant reduction of computation times compared with conventional time-domain simulation, which could allow optimization

procedures at the design stage of a power conversion system. Regarding the shielding issue of the cables, usually a well shielded cable is considered to help relieving the radiated EMI protection, but largely burdens the conducted EMI protection because of the extra shield capacitance C_S between the HV wires and the grounding. Besides, the termination of the cable shield should also be taken into account, since in [45] it is concluded that external input / output cable-shield termination has the greatest system EMC performance effect of all other design parameters.

The research regarding the modeling of the AC motor (including the motor capacitance C_W) can also be referenced by diverse of literature such as [3][4][5][7][8]. In [3], a high frequency model for induction motor based on lumped parameters has been proposed and a measurement procedure to obtain model parameters has been identified; while in [4] and [7], the EMC behavior of induction machines with power ratings from 370 W up to 45 kW is compared and a model library is set up for both frequency- and time-domain. The common-mode as well as differential-mode behaviors of the induction machines are also investigated by using the proposed simulation model and the relevant measurement results. In [8] it is confirmed that, the common-mode impedance of the induction motor can be considered as the capacitance C_g (in this dissertation designated as C_W in Fig. 2-7) coupling the winding to ground, which means that the path of common-mode current can be represented by this capacitance.

In this dissertation, since the focus of the research is located on the power semiconductor module, most discussions will be carried out regarding the coupling capacitance C_K (which is later divided into three parts e.g. C_+, C_- and C_{out}) in the following chapters, especially in chapter 5 and 6. The coupling capacitance C_K mainly comes due to the special construction of the DCB in the power module (see Fig. 2-11), which acts like a parallel plate capacitor with a ceramic layer in between two copper layers. The coupling capacitance can be affected by the construction of the heat-sink which is directly connected to the bottom copper layer of the DCB. Plenty of studies including simulations and measurements are already carried out regarding the influences on the EMC behavior in GHz range when the heat-sink geometry is modified [26][27][28][29], in which the heat-sinks are usually modeled as a solid block. In [30] it is found that the use of one common heat-sink creates the capacitive couplings which cause significant parasitic overshoots and oscillations and in return deteriorates the conducted EMI performance. Instead, the use of separated heat-sinks (between the multi half-bridges of the inverter) significantly reduces the EMI magnitudes especially for the DM noise. In addition, with the combined damping circuits the EMI performance is further improved. In [49] it is found out, in the power transmission system, if the rectifier module is separated from the heat-sink, the leakage current from the inverter module can no longer flow through the parasitic capacitances of the rectifier module back into the DC-link; instead it has to use the “protective conductor” and produces therefore a higher level of conducted EMI. The so called “protective conductor” means the electrical conductor (usually a flat copper strap) used in the active EMI measurement to ground the power module’s baseplate as well as the heat-sink, it is designated as “ground strap” in this dissertation and will be further researched and discussed in chapter 4.1.2, 5.2 and 5.3.

Generally, in order to reduce the conducted EMI which is caused by the above mentioned parasitic capacitances C_K, C_S and C_W, a well-known solution is to build the so-called Y-capacitors (usually combined with ferrite core) from the HV network (HV+, HV-) to the housing

of the power electronic systems [23][24][25]. However, their capacitance values are limited e.g. by the normative (leakage currents, contact protection) or functional requirements (no influence on the insulation monitoring, etc.).

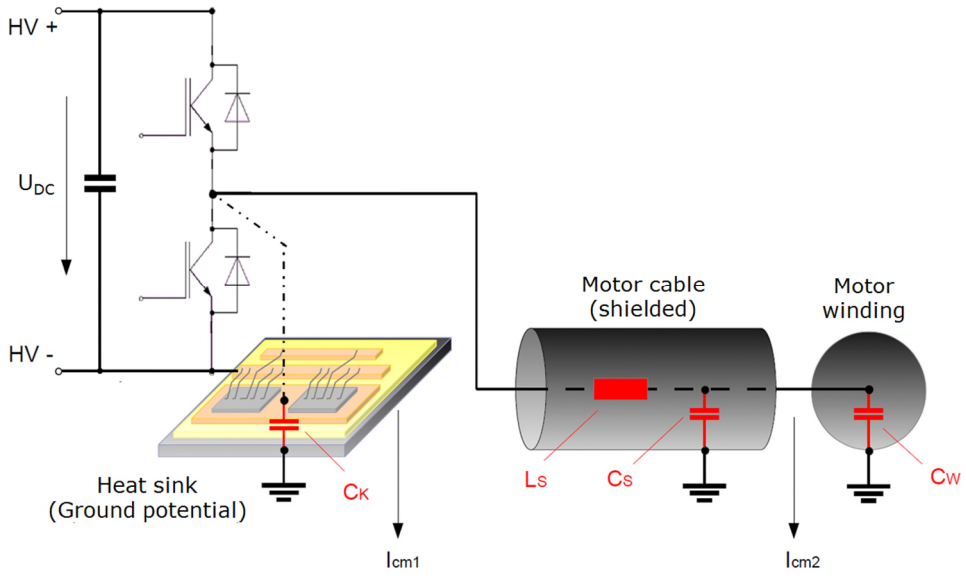


Fig. 2-7: Schematic representation of a commutation cell in power module and the coupling paths of the common-mode EMI (leakage currents I_{CM1} and I_{CM2}) via heat-sink and motor connection

2.1.3. EMI standards for industrial and automotive applications

Since the inverters with power module inside are used for equipment in a wide range of application fields including household appliances, industrial PDS (Power Drive System), automobile and traction system, it is imperative for the designers, as well as for the consumers, that the products comply with the stringent EMC regulations. By doing that, one can make sure that the products will not electrically disturb or being disturbed.

The IEC (International Electrotechnical Commission), which is a division of the ISO (International Organization for Standardization), is the most important international body for the EMC regulations. Within its technical committee structure, the IEC has two committees dedicated full time to EMC: the CISPR (International Special Committee on Radio Interference), which publishes standards related to the limits and methods of measurements for radiated and conducted interference; and the TC 77, whose publications deal with EMC between equipments, specifying electromagnetic environments, measurement techniques, emissions, inmmunity, etc. Although these international regulations are not mandatory, they serve as a foundation to the regulations created by other international organizations, national commisions, and manufaturers [60].

Within the United States the FCC (Federal Communications Commission) is in charge of the regulations of radio and wire communication, which include the control of the interference in such communications. The FCC rules and regulations are cointained in [61], and cover any device with timing pulses frequencies of at least 10 kHz. The devices are classified into two classes: 1) class A, for devices used in comercial, industrial, or bussines environment; and 2)

class B, for residential devices. The FCC regulations are compulsory, and it is illegal to market a device in the United States if it doesn't comply with them.

In Europe, the CENELEC (European Committee for Electrotechnical Standardization) is the European body in charge of producing EMC standards fo use with the European EMC directive, and it is made up of the national committees of each country. Once the CENELEC has produced an EMC European standard, all the member countries are required to implement identical national standards. The European EMC directive [75] harmonises the "generic standards" (for both emissions and immunity) as well as the "product standards". The generic standards such as EN61000-6-1...4 [62][63][64][65] are responsible to set out limits and test procedures, while the product standards such as EN61800-3 (for adjustable-speed electrical PDS) [66] etc. cover specific types of products.

The pulse frequencies of the PDS are often chosen in the range around (usually lower than) 10 kHz. For the harmonics in the frequency range of 150 kHz to 30 MHz, the product standard specifies different limits of the conducted emissions. To determine which of the limits are to be complied with, the standard defines two kinds of application environments of the PDS: On one side, the "first environment" is defined for the equipment which is connected directly to the low-voltage (less than 1000 V of AC RMS voltage, defined by IEC) power grid without an intermediate transformer, supplying power to buildings that are used for residential purposes (houses, apartments, shops or offices in residential buildings). In the first environment, the standard is further classified in Category 1 (C1) and Category 2 (C2), these two categories can be distinguished from each other by the concept "restricted / unrestricted distribution". That means, when the PDS is operated by a person without any EMC knowledge, the situation belongs to C1; when the person has EMC knowledge, it belongs then to C2. On the other side, the "second environment" is defined as the environment that contains all other facilities that are not directly connected to a low-voltage power grid which supplies power to buildings used for residential purposes. In the second environment, the standard classifies the Category 3 (C3) for the PDS with the rated voltage of less than 1000 V. In Fig. 2-8, the limits of the conducted EMI for the categories C1, C2 and C3 (here only for the PDS with a current consumption of less than 100 A) are presented.

From another point of view, in the generic standars EN61000-6-1...4, the specifications divides the applications into "industrial area" and "commercial area". By the conducted EMI emission limits, there are correlations between the product- and the generic-standards: The category C1 of the product standard correlates to the commercial area that is defined by the generic standard, while the categories C2 and C3 correlate to the industrial area.

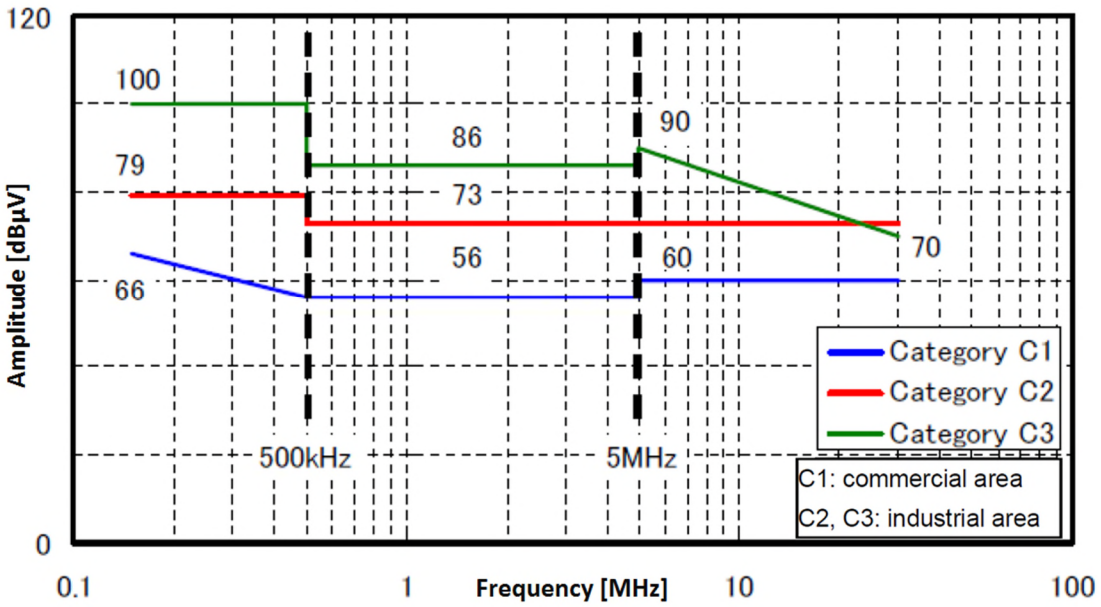


Fig. 2-8: Limits (Quasi-Peak values) of conducted EMI in product- and generic-standards

As for the automotive applications, the existing standard CISPR 25 [67] from IEC is considered to be the most relevant normative reference. The CISPR 25 applies to any electronic / electrical component intended for use in vehicles, trailers and devices; it contains limits and procedures for the measurement of radio disturbances in the frequency range of 150 kHz to 2.5 GHz. The limits are intended to provide protection for receivers installed in a vehicle from disturbances produced by components / modules in the same vehicle. The receiver types to be protected are, for example, broadcast receivers (sound and television), land mobile radio, radio telephone, amateur, citizens' radio, satellite navigation (GPS etc.) and Bluetooth. Since the mounting location, vehicle body construction and harness design can affect the coupling of radio disturbances to the on-board radio, the CISPR 25 defines multiple limit levels. For example, the Quasi-Peak levels of conducted EMI for components / modules in the vehicle are defined in 5 classes in the frequency range of 150 kHz to 108 MHz (Fig. 2-9 and Table 1). The level class to be used (as a function of frequency band) shall be agreed upon between the vehicle manufacturer and the component supplier (meaning the power module manufacturer in this dissertation). The diverse discontinuous frequency bands that are defined in Table 1 are not applicable to all regions or countries of the world. For economic reasons, the vehicle manufacturer must be free to identify what frequency bands are applicable in the countries in which a vehicle will be marketed and which radio services are likely to be used in that vehicle [67].

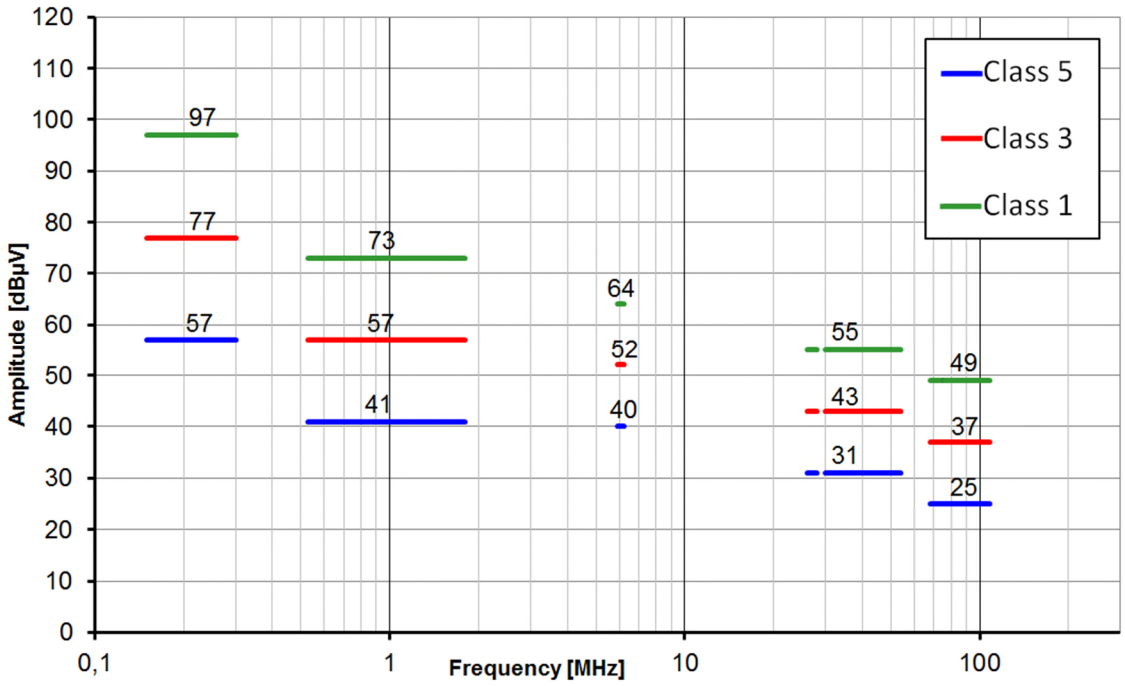


Fig. 2-9: Limits (Quasi-Peak values, voltage method) of conducted EMI in standard CISPR 25 for components / modules in automotive application

Table 1: Quasi-Peak levels (voltage method) of conducted EMI for components / modules of the vehicle in standard CISPR 25

Service / Band	Frequency [MHz]	Quasi-Peak levels [dBµV]				
		Class 1	Class 2	Class 3	Class 4	Class 5
Broadcast						
LW	0.15 - 0.30	97	87	77	67	57
MW	0.53 -1.8	73	65	57	49	41
SW	5.9 - 6.2	64	58	52	46	40
FM	76 -108	49	43	37	31	25
Mobile Services						
CB	26 -28	55	49	43	37	31
VHF	30 -54	55	49	43	37	31
VHF	68 -87	49	43	37	31	25
LW: Long wave, MW: Medium wave, SW: Short wave (amplitude modulation, AM) FM: Frequency modulation CB: Cell Broadcast VHF: Very high frequency						

The measurement results of high-frequency EMI are often influenced by many external factors during the course of the measurement. In order to prevent or minimize such influences, the

measurement setups for the conducted and radiated EMI are normalized respectively by the standard CISPR16-1 for industrial application as well as the standard CISPR 25 for automotive application. Principally the measurement setups for the both kinds of applications don't quite differ from each other. Usually the following components are essential parts of the conducted EMI test bench:

- Power supply
- Artificial network (LISN)
- DUT (power semiconductor module in this dissertation)
- Load (real motor or simulator)
- Power supply lines
- Load wires / cables
- Ground plane
- Shielded enclosure
- Measuring instrument (Scanning receiver or spectrum analyzer)

The specifics of the components, such as their materials, their locations, their parameters and the test procedures etc. are respectively defined in each standard depending on the industrial or automotive applications. The conducted emission measurement generally includes two kinds of methods: the voltage method and the current probe method. Although it can characterize the emissions on single leads only, yet the voltage measurement is the most frequently used method because of its simple and normalized setup. For both of the measurement methods, to be able to correlate the measured data between different measurements sites, the impedance seen by the DUT, and over which these measurements are made, has to be stabilized from site to site. Therefore, a normative AN (Artificial network) which is also named as the LISN (Line Impedance Stabilization Network) is needed. The use of the LISN during the conducted EMI measurements serves mainly two purposes: 1) to prevent external conducted noise (from the power lines) from contaminating the measurements and, 2) to present constant impedance between the grounding and the power line, making sure that the measurements are reproducible [15]. The schematic representation of a single phased LISN is shown in Fig. 2-10. The presence of the capacitor C_1 and the inductor L_1 is to divert the external noise from the power supply, preventing them from contaminating the EMI measurement results over the tested frequency ranges. The 50 Ω resistor represents the input impedance of the measuring instrument. The capacitor C_2 is constructed to prevent any DC voltage from overloading the measuring instrument. The resistors R_1 and R_2 serve to discharge the capacitors C_1 and C_2 in case the 50 Ω resistor is removed. The values of these passive components in the LISNs for industrial and automotive applications are compared to each other in Table 2.

Table 2: Comparison of the parameters in LISN for industrial / automotive applications

Application field	L_1 [µH]	C_1 [µF]	C_2 [µF]	R_1 [Ω]	R_2 [Ω]
Industrial	50	8	0.47	5	1000
Automotive	5	1	0.1	0	1000

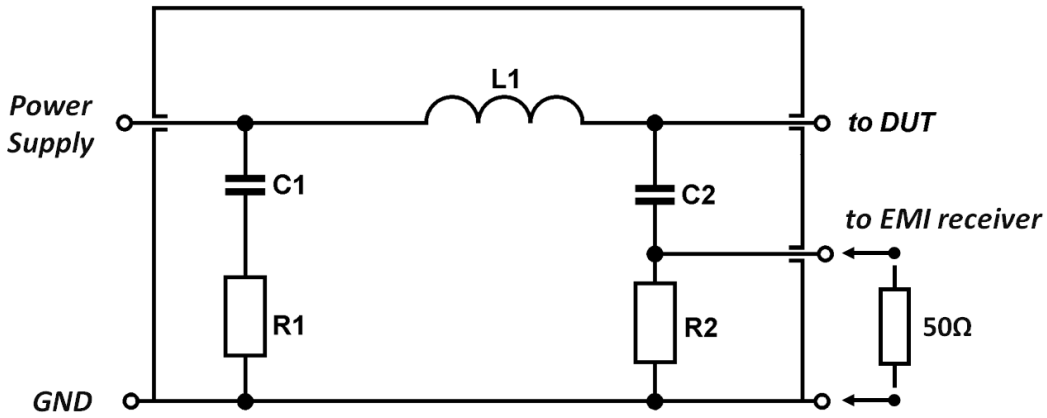


Fig. 2-10: Schematic of single phase LISN in the drive system for EMI measurement

2.2. Switching behavior of semiconductors and its characterization

Since the switching operation of the power semiconductors is regarded as the main cause of the EMI, the switching characteristics of the IGBT and diode shall be considered more specifically. In this chapter, the relevant basic knowledge about the dynamic performances of the semiconductors within the power module are indroduced. After that, the manner of the measurements in laboratory, whereby the dynamic characteristics of the semiconductors in power module can be investigated, are presented. These measurement methods and setups will be used to characterize the switching performance of the EMI-optimized power modules in the chapter 6 of this dissertation.

2.2.1. IGBTs and diodes in power modules

The discussion regarding the switching behavior of the power semiconductor chips (IGBTs and diodes) without considering their packaging is less meaningful, because the construction and connection of the chips can bring additional parasitic components, which significantly impact or limit the power semiconductors' dynamic and static performances.

In order to fulfill the demands of various output power densities, the power semiconductor chips are usually assembled in discrete form, disc-cell or module. Nowadays most modules are built up through various combinations of soldering and bonding processes. The realization of these processes can be summarized in Fig. 2-11: The top and bottom sides of each silicon chip provide contacts with a thick metal layer of approximately 5 µm. Bonding wires are applied on the top side of the chip, while the chip's bottom side is connected to the substrate via solder joints. The substrates differ essentially in their production processes. Typically used substrates are Direct Copper Bonded (DCB) or Active Metal Brazed (AMB). In these, copper or aluminum are combined with aluminum oxide or aluminum nitride ceramic to form a layer structure. The

top side copper is then patterned by an etching processes to generate different tracks. The benefit of the ceramic and copper substrate is that its thermal expansion coefficient is close to that of silicon. Due to the ceramic insulation layer, the power module has two major advantages: Firstly, this insulating layer separates the voltage level inside the module from the heat sink (basic insulation) and thus allows the trouble-free installation of several modules on the same heat sink; Secondly, this isolation allows the operation of components at different potential levels (functional insulation) [72]. The DCB substrate used in this dissertation is usually made of aluminum oxide (Al_2O_3) with approximately 300 µm thick copper layers on both sides. The contacting of the semiconductor chip top side is realized by bonding processes with aluminum wire, recently also copper wire.

The advantages of the power modules are, on the one hand, the possibility of structuring the upper copper layer of the DCB as a conductive pattern, which enables the electrically isolated construction of a complete circuit (e.g., three-phase inverter) in one module; on the other hand, the simplicity of the installation.

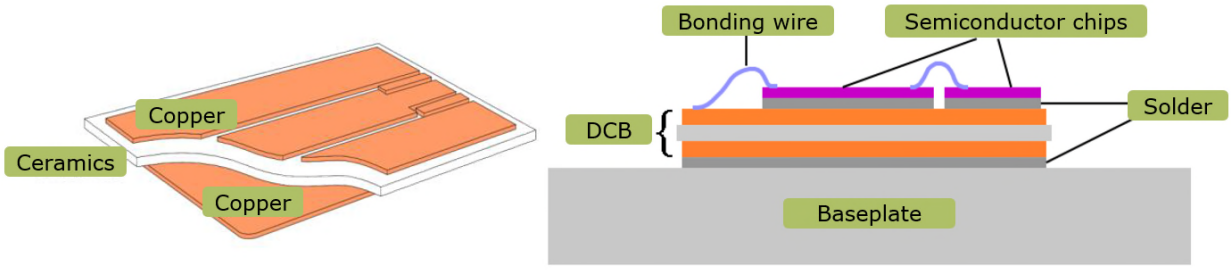


Fig. 2-11: Constructions of DCB (left) and power module without frame (right) in sectional view

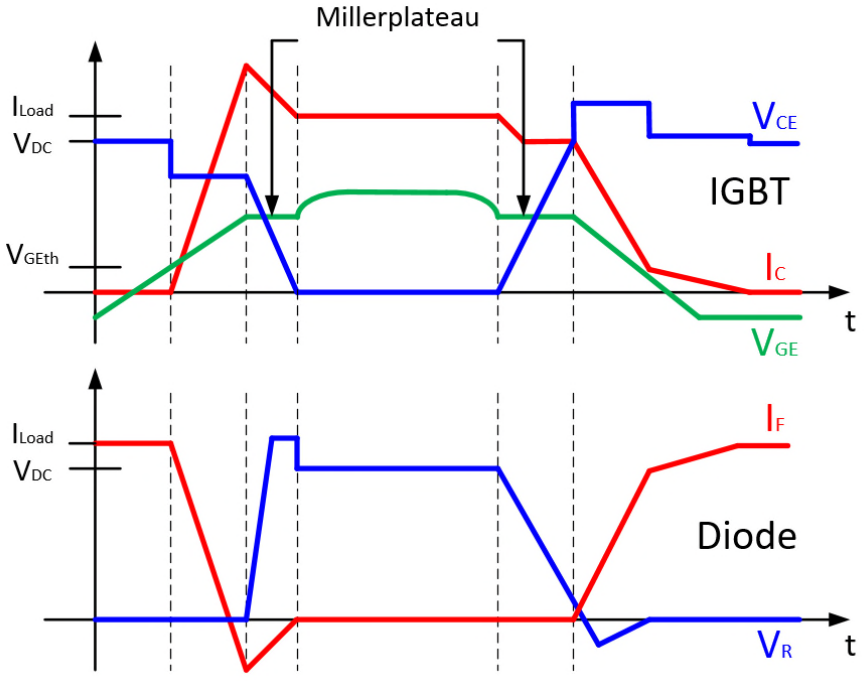


Fig. 2-12: Switching-on and -off performances of IGBT and diode in power module

The IGBT is controlled by the gate voltage V_{GE}. If the gate voltage is negative, it stays in the off state. As soon as the gate voltage reaches the threshold voltage V_{GEth}, the IGBT becomes conductive and the load current can commute from the diode to the IGBT. In addition to the load current, the IGBT takes over the reverse recovery current of the free-wheeling diode and carries a current peak during the turn on process. According to the law of induction by $\Delta V_{CE} = L \cdot \frac{dI_C}{dt}$, the current change rate dI_C/dt causes a voltage drop at the module's parasitic inductances in the commutation cell. This voltage drop counteracts the driving DC-link voltage V_{DC} and is visible as a voltage dip in the collector-emitter voltage V_{CE}.

After reaching the reverse recovery current peak, the diode can take over the reverse bias and the reverse current starts to drop. Only then the voltage on the IGBT can decrease. The decreasing voltage dV_{CE}/dt causes an additional current in the parasitic capacitances of the commutation cell, which overlaps with the IGBT current I_C. During this time, the drop of the diode's reverse current with a certain rate of dI_F/dt can lead to an overvoltage which burdens the diode itself (as well as its parallel IGBT at the same side of the half-bridge). At the same time, the gate-collector capacitance (Miller capacitance) must be recharged. The gate-emitter voltage V_{GE} remains constant during the recharging period and thereby forms the so-called Miller plateau. When the diode has taken over the entire blocking voltage, the gate voltage rises to its final value and the static turn-on state is reached.

By receiving the turn-off command, the gate voltage drops to the Miller plateau. During the plateau, the IGBT takes over the voltage drop again. Meanwhile, the voltage across the diode decreases. According to the equation $\Delta I_C = C \cdot \frac{dV_{CE}}{dt}$, the changing voltage dV_{CE}/dt causes an additional current in the parasitic capacitances of the commutation cell, that is visible as a current dip in the collector-emitter current I_C.

The diode can start to take over the current only when the entire blocking voltage drops across the IGBT. The commutation current's steepness dI_C/dt has an opposite sign during turn-off and turn-on. Therefore, the blocking voltage across the IGBT is increased due to the additionally induced voltage caused by the stray inductances of the whole commutation path. Thus, an overvoltage peak is formed during the turn-off process. After that, the minority carriers in the IGBT must be removed from the device, which causes a collector current tail.

As mentioned before, the impact of the semiconductor chips' construction and connection in the power module are critical. The switching curves V_{CE} (resp. V_R) and I_C (resp. I_F) can deviate strongly from ideal trapezoidal curves due to parasitic elements. If the dimension of the parasitic elements in the power module is changed, the reshaped switching characteristics are directly visible. For example, at the same operation point, reducing the stray inductances in the commutation cell can lead to proportional decrease in the voltage drop during the IGBT turn-on as well as reduced overvoltage peak during the IGBT turn-off [18]. Furthermore, from the emission point of view, stray inductances are of particular importance by investigating the EMI of inverters, since, given certain values in combination with parasitic capacitances from the power module or from the drive system, they can lead to resonance in the HV circuit and excite oscillations.

2.2.2. Characterizing the switching behavior through double-pulse measurements

In order to characterize the switching behavior of the IGBT and diode, proper dynamic measurements in the laboratory are necessary. The preferred measurement method in this dissertation is called the “double-pulse test”. This measurement method is widely used by the power semiconductor manufacturers because of its simplicity and reproducibility during its implementation.

The double-pulse test can be described as follows: During the test, the IGBT in one side of the power module’s half-bridge is turned on and off twice. Fig. 2-13 shows the typical voltages (V_{CE} and V_{GE}) as well as current (I_C) profiles during the measurement. The first pulse allows the load current flowing through the switching IGBT to build an initial status. This pulse must be long enough in order to ensure that the IGBT reaches a steady state in conducting direction, and be as long as needed (in the test usually between 50 µs to 100 µs), so that the needed magnitude of the current flow is reached, before the IGBT turns off. After that, the IGBT must remain in off state until the free-wheeling diode has reached steady state of conduction (in the test usually set to 100 µs). Then, the IGBT is turned on once again for a short while (approx. 15 µs) until the voltage V_{CE} has decreased to the collector-emitter saturation voltage V_{CEsat} before finally turning off, by which point the whole test process is completed. From the characterization point of view, the IGBT switching off behavior is recoded at the end of the first pulse; the IGBT switching on as well as the reverse recovery behavior of the free-wheeling diode are recoded at the beginning of the second pulse.

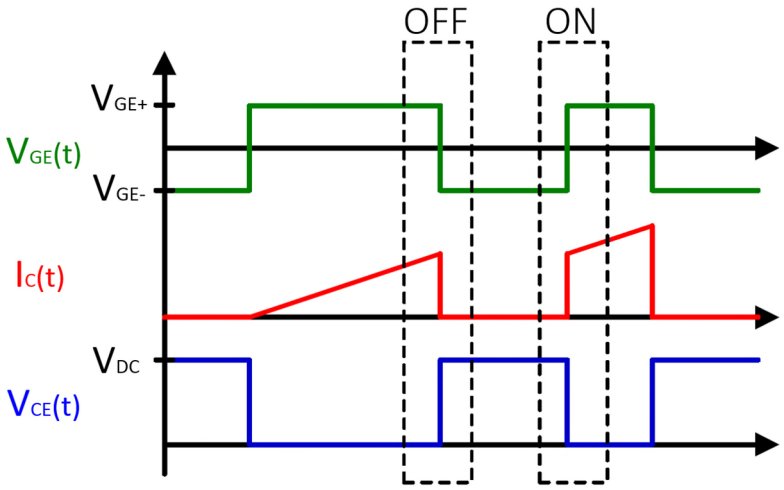


Fig. 2-13: The course of the double-pulse test

To realize the double-pulse characterization, the power module with the semiconductors inside as the DUT is basically operated under a buck converter mode. That means, the IGBT in one side of the half-bridge is connected in series with an external inductive load (mostly a coil) and controlled by the gate signals to switch on / off, while the diode in the other side of the half-bridge is working as a free-wheeling diode to conduct the load current intermittently. The schematic for the measurements of the IGBT (from low side of the half-bridge) and of its free-wheeling diode (from high side of the half-bridge) is presented in Fig. 2-14. Depending on the connected position of the oscilloscope’s grounding, a transformer between the grid and the

power supply may be necessary to separate the tested high voltage system from the general GND.

For the trials in this work, the inductive load is connected between the positive node of the DC-link and the AC output (also possible between DC- and AC node, depending on which side of the semiconductor is measured), resulting in a parallel connection with the HS IGBT which stays constantly in OFF state. The LS IGBT is connected and controlled by an Infineon® driver board. This so called “EV-driver” can generate an output voltage from the positive rail to GND by 0.6 V to 28 V. From the negative rail to GND, it can be 0 V to -20 V. Furthermore, the driver has 8 switching stages in which 8 R_{gon}s and 8 R_{goff}s can be switched separately from each other. The driver itself is supplied with a DC voltage of 15 V. The switching pulse comes via a fiber optic cable and is converted by the driver into an electrical signal to output. Thus there is no microcontroller on the driver itself that generates the switching pulse. To select the switching stage and the voltage, an Ethernet connection to a PC is required. The driver configuration is then done via a Labview-tool. The capacitor used for the DC-link is the EPCOS® film capacitor *B25655J4507K*, with a capacitance of 500 µF, ESR of approx. 1 mΩ, and ESL of approx. 15 nH [71]. The power module and the capacitor bus bar are connected through flat terminals with screws, resulting in short paths with low stay inductances of less than 10 nH per line. According to [73], minimum parasitic inductance allows improving power semiconductors towards lower losses. The oscilloscope WaveRunner HRO 66Zi from LeCroy® is used to record the switching curves; it has a maximum sampling rate of 2 GHz, and a sensitivity of up to 1 mV/div. The vertical resolution of the oscilloscope is 12 bits. The currents flowing through the IGBT or the diode are measured with a PEM® CWT Rogowski coil probe (CWT15), which is mounted around the terminals connecting the DC-link with the power module. The high voltage drops V_{CE} or V_R are measured with the PMK® high voltage probe PHV 1000 with the probe factor of 100. The gate-emitter voltage V_{GE} of the active IGBT is usually measured with the Tektronix® passive probe P6139B. If the auxiliary emitters (AE) used for the V_{CE} and V_{GE} measurements are from different sides of the half-bridge, a TESTEC differential probe (TT-SI 9110) can be used for either V_{CE} or V_{GE} measurement (This unusual situation is not covered in the schematic below).

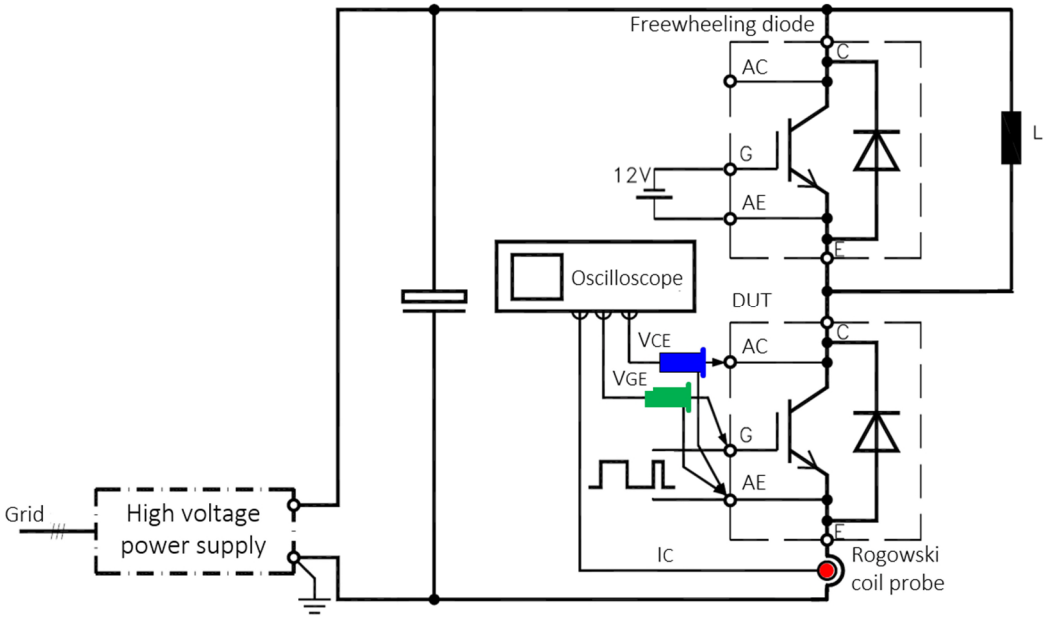


Fig. 2-14: Schematic for IGBT measurement in the double-pulse test

3. Investigations about the EMI source

The use of fast switching devices (such as IGBTs) in PWM inverters causes EMI problems in the drive system or grid respectively. The generated high voltage slew rate $\mathrm{dv/dt}$ and high current slew rate $\mathrm{di/dt}$ during the switching processes have been established as the main source of EMI in electrical applications [9].To characterize the EMI of the inverter, it is meaningful to focus on the device switching effects at first.

3.1. FFT analysis of unideal switching edge

As explained in chapter 2.1.1, the switching frequency related output voltages of power modules as well as their commutation currents are approximated as pulse-shaped with simplex rising and falling edges. In this dissertation, for better approaching of the output voltage, the researched object is a deformed trapezoidal pulse in time-domain, by which an extra plateau with constant amplitude is added into the rising edge of the trapezoid. The reason for choosing this kind of pulse to study can be explained as follows: During the operation of the inverter respectively the power module, the shape of the output voltage (U_{AC}) is changing. The steepness of the rising edges is affected by the load current and the stray inductance of the construction. The origin for this effect will be discussed and explained in detail in 3.2.2. In this sub-chapter we only focus on the mathematical discussion of the influences in frequency-domain that are brought by the deformation of the trapezoidal pulse. As presented in Fig. 3-1, the deformed rising edge of the output voltage can be approximated by a constant rising edge with an inserted plateau. The approximated rising edge can be combined with a falling edge with constant steepness and form a deformed trapezoidal pulse, which is called “trapezoid with plateau” in this dissertation.

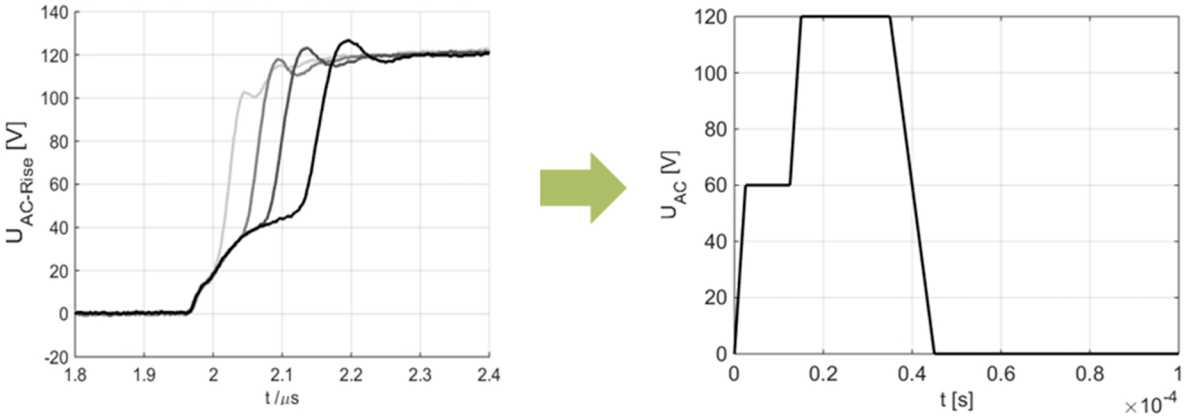


Fig. 3-1: Measured deformed rising edges of the output voltage in power module (left) and the approximation by the "trapezoid with plateau" (right)

In order to compare the spectrums of the trapezoidal pulses with and without plateau, the maximum spectrum limits of the trapezoid with plateau shall be found out first. The trapezoid with plateau in time-domain can be taken apart into two standard trapezoids with half of the amplitude. As shown in Fig. 3-2, the target shape in black with a plateau of t_p and amplitude of A can be considered to consist of the 1st trapezoid in green combined with the 2nd trapezoid in red. The two sub-trapezoids with different average durations are superimposed on each other. To simplify the calculation, the durations of the rising and falling edges for each sub-trapezoid are set to be $\frac{R}{2}$ and $\frac{F}{2}$, respectively half of the target shape. The segmented functions of each shape are defined in Table 3. The parameters are normalized and marked with an apostrophe: $t' = t/T$, $M' = M/T$, $R' = R/T$ and $F' = F/T$ and $t'_p = t_p/T$.

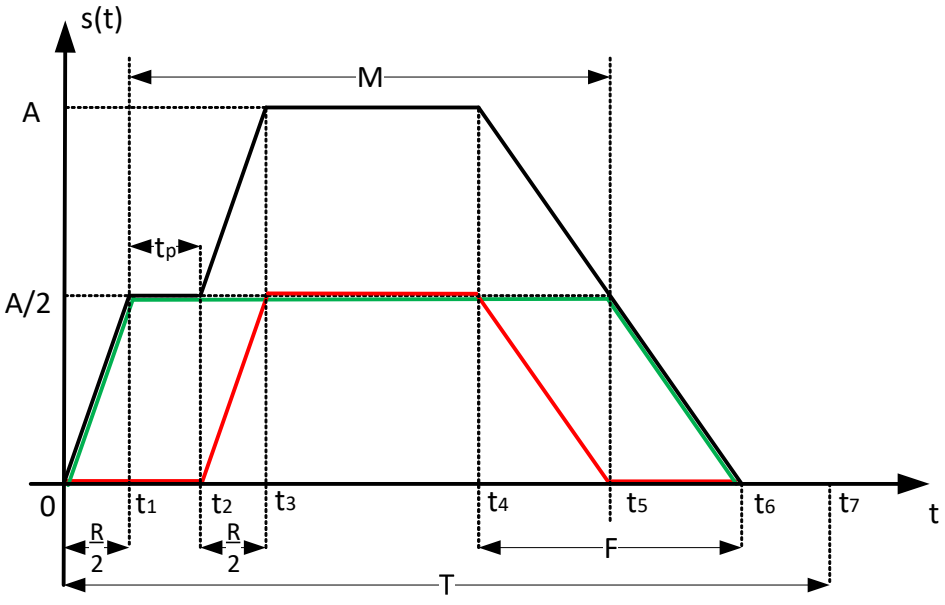


Fig. 3-2: Decomposition and parameterization of the target trapezoid with plateau (black) into two sub-trapezoids (green and red) in staggered position

Table 3: Defining the segmented functions of the trapezoid with plateau and its two sub-trapezoids

<table>
<tr><td rowspan="2">Section</td><td colspan="3">Function s(t')</td></tr>
<tr><td>Trapezoid with plateau</td><td>1st sub-trapezoid</td><td>2nd sub-trapezoid</td></tr>
<tr><td>$0 \leq t' < t'_1$</td><td>$\frac{A}{R'}t'$</td><td>$\frac{A}{R'}t'$</td><td rowspan="2">0</td></tr>
<tr><td>$t'_1 \leq t' < t'_2$</td><td>$\frac{A}{2}$</td><td rowspan="4">$\frac{A}{2}$</td></tr>
<tr><td>$t'_2 \leq t' < t'_3$</td><td>$\frac{A}{R'}(t' - t'_p)$</td><td>$\frac{A}{R'}\left(t' - t'_p - \frac{R'}{2}\right)$</td></tr>
<tr><td>$t'_3 \leq t' < t'_4$</td><td>A</td><td>$\frac{A}{2}$</td></tr>
<tr><td>$t'_4 \leq t' < t'_5$</td><td rowspan="2">$\frac{A}{F'}\left(\frac{R'}{2} + M' + \frac{F'}{2} - t'\right)$</td><td>$\frac{A}{F'}\left(\frac{R'}{2} + M' - t'\right)$</td></tr>
<tr><td>$t'_5 \leq t' < t'_6$</td><td>$\frac{A}{F'}\left(\frac{R'}{2} + M' + \frac{F'}{2} - t'\right)$</td><td rowspan="2">0</td></tr>
<tr><td>$t'_6 \leq t' < t'_7$</td><td>0</td><td>0</td></tr>
</table>

By using the methods that are presented in [5] for the approximation of the spectrums, the segmented functions in frequency-domain of the approximated spectrums can be listed in Table 4, compared to that of a standard trapezoidal pulse. For frequencies in the range of the switching frequency $\frac{1}{T}$ (respectively $f < f_{k1}$ in Fig. 2-4), the spectrum can be determined by the value of the switching frequency, by assuming that $k = 1$ ($k = fT$) in the equation (2-3). In this first section of the function S(f) in Table 4, the spectrums remain approximately constant, the steepness of the approximated lines correspond to 0 dB / decade. Compared to a standard trapezoid for reference, the average durations of the two sub-trapezoids' pulses are different. That means, the average duration of the 1st sub-trapezoid is extended by $\frac{R'+F'}{4}$, while that of the 2nd sub-trapezoid is reduced by $-(\frac{R'+F'}{4} + t'_p)$.

For the frequencies above the first harmonic, an approximation can be found by considering that for small k the arguments of the si-functions remain small. Thereby the envelope lines of the spectrums for the second sections will fall with 20 dB / decade.

The knee frequency f_k represents the intersection point of the first two approximation lines. By the target trapezoid with plateau, there are 2 knee frequencies f_{k1_1} and f_{k1_2} to take into account, since the average durations of the two sub-trapezoids differ from each other. For the trapezoid without plateau, the "worst-case" of the spectrum always appears when the duration M is half of the pulse period T, respectively $M' = 0.5$, since the sin-function oscillates between +1 and -1. For the target trapezoid with plateau, if the average duration M, the rising time R and the falling time F as well as the plateau t_p are very small in comparison with the entire

pulse period T, then the expression of the two knee points of the approximation line can be simplified to equation (3-1).

$$f_{k1\_1} = \frac{1}{\sin\left[\pi\left(M' + \frac{R'+F'}{4}\right)\right]T} \approx \frac{1}{\pi\left(M' + \frac{R'+F'}{4}\right)T}$$
$$f_{k1\_2} = \frac{1}{\sin\left[\pi\left(M' - \frac{R'+F'}{4} - t_p'\right)\right]T} \approx \frac{1}{\pi\left(M' - \frac{R'+F'}{4} - t_p'\right)T} \quad \textbf{(3-1)}$$

Before the first knee point f_{k1_1} is reached, the function of the target trapezoid (with plateau) can be expressed as the sum of the two approximation lines with the steepness of 0 dB / decade from each of the sub-trapezoids. After the first knee point f_{k1_1}, before the second knee point f_{k1_2} is reached, the function of the target trapezoid consists of the first section of the 2nd sub-trapezoid (with the steepness of 0 dB / decade) combined with the second section of the 1st sub-trapezoid (with the steepness of 20 dB / decade). After that, the approximation line will fall with a rate of 20 dB / decade until the third knee point of $f_{k2} = \frac{2}{\pi\alpha T}$ is reached. In this expression, α is the larger one of R' and F', respectively the smoother slope of the rising- and falling-edge, while β is the smaller one of R' and F' respectively the steeper slope of the rising- and falling-edge. These combinations are listed in Table 5.

For the frequencies where $k \cdot R'$ or $k \cdot F'$ is significantly greater than 1 in the argument of the si-functions ($si(x) = \frac{\sin(x)}{x}$), the upper limit of the si-function in equation (2-3) converges to $\frac{1}{\pi k R'}$ or $\frac{1}{\pi k F'}$. The reduction of the spectrums in this phase will be much more rapid than the phases before. Two further approximation lines with slopes of -30 dB / decade and -40 dB / decade can be observed in Fig. 3-3. Since the rising- and the falling-time generally differ from each other (thus also the normalized parameters R' and F'), there will be a frequency range in which one of the two si-functions converges to 1, while the other already converges to $\frac{1}{\pi k \alpha}$. That means the section for 30 dB / decade between the knee points f_{k2} and f_{k3} will be determined by the smoother edge of the trapezoidal pulse. In the target trapezoid with plateau, since it has been assumed that the steepness (of the rising edge) before and after the plateau keeps unchanged, the knee points f_{k2} and f_{k3} for both of the sub-trapezoids shall be the same. Compared to the reference trapezoid, if a plateau is inserted in the rising edge, the value of the knee points f_{k2} and f_{k3} will respectively double because each rising- and falling-time (R' and F') of the its sub-trapezoids are halved.

Table 4: Functions in frequency domain for the approximation of the spectrums for trapezoidal impulses

Section	Function S(f)		
	Trapezoid (Ref.)	1st sub-trapezoid	2nd sub-trapezoid
0dB / decade	$\frac{2A}{\pi}\sin(\pi M')$	$\frac{A}{\pi}\sin\left[\pi\left(M'+\frac{R'+F'}{4}\right)\right]$	$\frac{A}{\pi}\sin\left[\pi\left(M'-\frac{R'+F'}{4}-t_p{}'\right)\right]$
−20dB / decade	$\frac{2A}{\pi k}$	$\frac{A}{\pi k}$	$\frac{A}{\pi k}$
−30dB / decade	$\frac{A}{\pi k}\left(1+\frac{1}{\pi k\alpha}\right)$	$\frac{A}{2\pi k}\left(1+\frac{2}{\pi k\alpha}\right)$	$\frac{A}{2\pi k}\left(1+\frac{2}{\pi k\alpha}\right)$
−40dB / decade	$\frac{A}{\pi^2k^2}\left(\frac{1}{R'}+\frac{1}{F'}\right)$	$\frac{A}{\pi^2k^2}\left(\frac{1}{R'}+\frac{1}{F'}\right)$	$\frac{A}{\pi^2k^2}\left(\frac{1}{R'}+\frac{1}{F'}\right)$

Table 5: Segmented functions and knee frequencies for the approximation of the spectrum for the target "trapezoid with plateau"

Section	Function S(f)	Knee frequency f_k (end of each section)
0dB / decade	$\frac{A}{\pi}\left\{\sin\left[\pi\left(M'+\frac{R'+F'}{4}\right)\right]+\sin\left[\pi\left(M'-\frac{R'+F'}{4}-t_p{}'\right)\right]\right\}$	$f_{k1\_1}=\frac{1}{\pi\left(M'+\frac{R'+F'}{4}\right)T}$
Between 0dB and −20dB / decade	$\frac{A}{\pi}\left\{\frac{1}{k}+\sin\left[\pi\left(M'-\frac{R'+F'}{4}-t_p{}'\right)\right]\right\}$	$f_{k1\_2}=\frac{1}{\pi\left(M'-\frac{R'+F'}{4}-t_p'\right)T}$
−20dB / decade	$\frac{2A}{\pi k}$	$f_{k2}=\frac{2}{\pi\alpha T}$
−30dB / decade	$\frac{A}{\pi k}\left(1+\frac{2}{\pi k\alpha}\right)$	$f_{k3}=\frac{2}{\pi\beta T}$
−40dB / decade	$\frac{2A}{\pi^2k^2}\left(\frac{1}{R'}+\frac{1}{F'}\right)$	…

As a summary of the calculations and analysis, considering a trapezoidal pulse with a flat plateau inserted into its rising edge, without affecting the original steepness of the edge, the following changings will happen regarding the spectrum of the deformed trapezoidal pulse:

- In low frequency area near to the fundamental frequency before the first knee point f_{k1_1} is reached, by $M' \ll 0.5$, the amplitude of the target spectrum will always be slightly smaller than that of the trapezoid without a plateau inserted. The longer the plateau lasts, the

larger this difference is to be seen. However, this difference turns out to be almost invisible when $M' \approx 0.5$.

- In middle frequency area by which the spectrum drops with -20 dB / decade and -30 dB / decade, the amplitude of the target spectrum shows almost no difference than that of the trapezoid without a plateau.
- In high frequency area by which the spectrum drops with -40 dB / decade, the last knee point f_{k3} will be twice as large as that of the trapezoid without a plateau, and thus the amplitude of the target spectrum is 6 dBµV higher.

These conclusions can be observed in Fig. 3-4 through the comparison of the trapezoids with / without plateau inserted. In the diagrams, the approximation lines of the spectrums are verified by the FF-transformed spectrums of the time-domain pulses on the left side (in blue and red). As expected, in the low frequency area, the spectrums in blue and red don't differ from each other much; In the high frequency area after the last knee point, the blue line is constantly 6 dB higher than the red line.

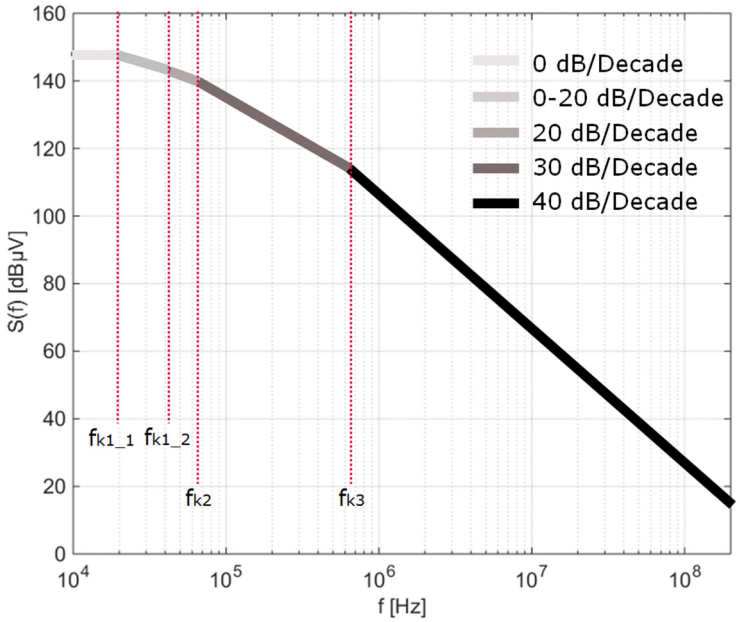


Fig. 3-3: Five envelope lines with different steepness and knee points for the spectrum approximation of the pulse "trapezoid with plateau"

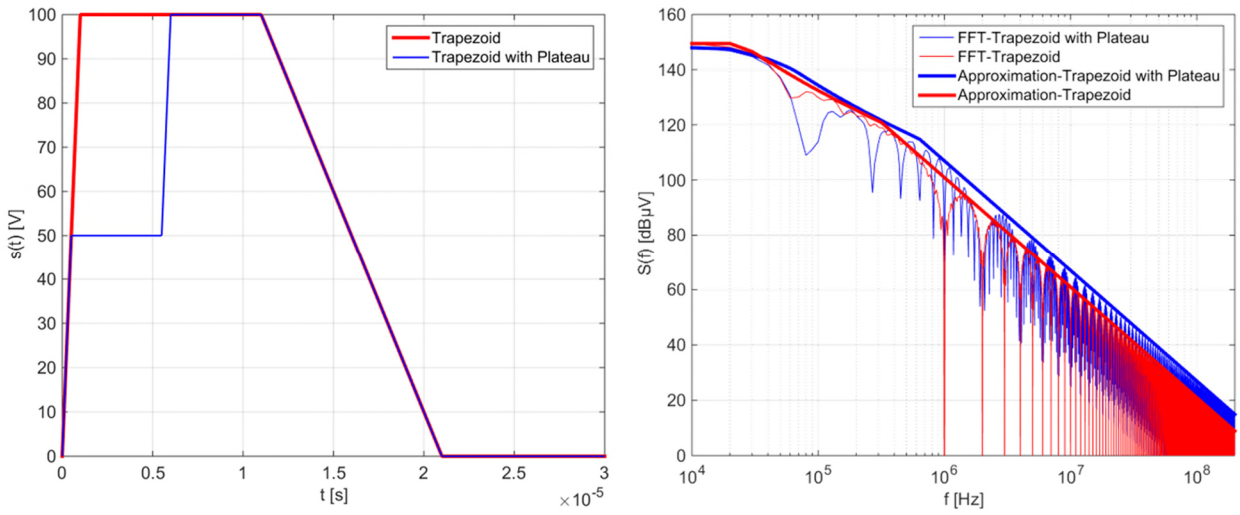


Fig. 3-4: Comparison of the trapezoids with / without plateau

3.2. EMI differences in buck-converter and inverter operations by considering the DRR effects

In the conducted EMI measurements, different from a three-phase inverter operating mode, the power modules are usually operated in a buck-converter mode to provide a simplified testing setup [10][11][74]. The justification for doing this runs as follows: Each switching event in an inverter involves an IGBT and a diode on the same phase leg; a clear understanding of the EMI noise generation mechanisms of a single-phase leg is necessary and can lead to understanding the entire multi-phase inverter [10][12].

However, such simplification has certain disadvantages. Fig. 3-5 shows that despite using the same measurement conditions (e.g. DC-link voltage, load current (RMS value), switching frequency, etc.), the measured EMI of a buck-converter operation are lower than the EMI of an inverter operation. It can be observed from the figure, that the shape of the inverter operation spectrum looks like the envelope of the buck-converter operation spectrum. The reason is that the duty-cycle [21] of the PWM signal is inconstant during the inverter operation, which causes a shift of the ripple and an overlap in the spectrum so that an envelope effect emerges. By EMI average-measurement up to 30 MHz, a difference between the conducted emissions (approx. up 2 to 10 dBµV) originating from the inverter operation and from the buck-converter operation has been observed above approx. 2 MHz. The reasons for this deviation are investigated in this chapter.

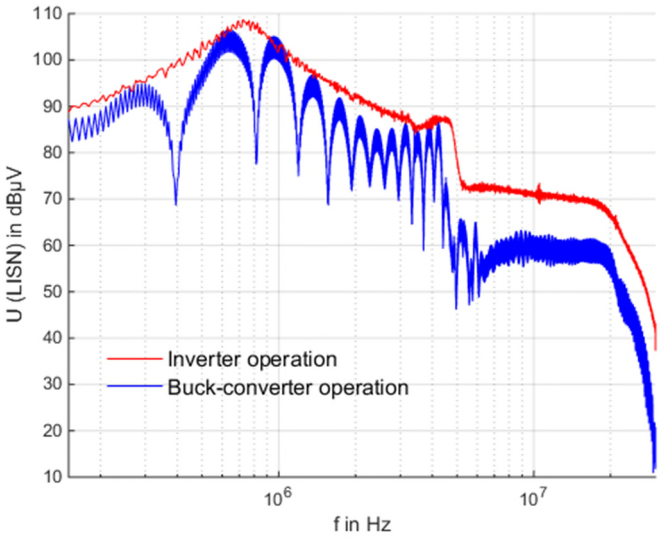


Fig. 3-5: EMI spectrum (in average) of two operation modes using the same measurement conditions, i. e., $I_{DC,buck}$=$I_{RMS,inv}$ (V_{DC}=100V, I_{RMS_Load}=50A, f_{switch}=10kHz)

3.2.1. Effect of DRR on switching edges

As introduced before, a study of the high voltage slew rate dv/dt during the switching actions is necessary for the EMI study. The voltages at the middle point of a half-bridge (U_{AC}) are measured against ground (GND) during the IGBT switching. The changing dv/dt at this point is normally considered as a critical interference source of the common-mode EMI in power modules [1].

The measurement results indicate that there are two types of rising as well as falling edges at this point (Fig. 3-6): The rising and falling edges with relatively steep slopes (approx. 2kV/µs) are drawn in red, as well as the rising and falling edges with relatively gentle slopes (approx. 400V/µs) are drawn in blue. The curves are marked “With or without DRR (Diode Reverse Recovery effect)”, because the DRR effects are involved in these switching processes [77]. The DRR effects are widely recognized as a cause of EMI generation in hard-switched power converters [13][14].

The mechanisms of producing the edges with different slopes are explained as follows: The edge with the low dv/dt (blue) is produced by the normal free-wheeling process of the diode (Fig. 3-9 and Fig. 3-10), while the edge with the high dv/dt (red) comes due to the DRR process (Fig. 3-7 and Fig. 3-8). Taking the rising edges of U_{AC} in Fig. 3-7 and Fig. 3-9 as example, when the HS (high side) switch is off, the LS (low side) diode is conducting the load current (status 1). If the HS switch receives a gate signal and turns on again, the DRR of the LS diode occurs for a short while (status 2) and the load current commutates to the HS switch to flow continuously (status 3). During this transition from status 1 to 3, a steep rising edge is built up between the middle point of the bridge and the ground. The edge turns to be gentler, if the current commutates to the diode turning off the LS IGBT, which is illustrated in Fig. 3-9. In status 6, the LS switch is driven by the gate signal and turns off. The load current is forced

to flow through the HS diode of the same bridge (status 4) and causes a free-wheeling process. A relatively gentle edge of U_{AC}, compared with the situation in Fig. 3-7, is built up thereby.

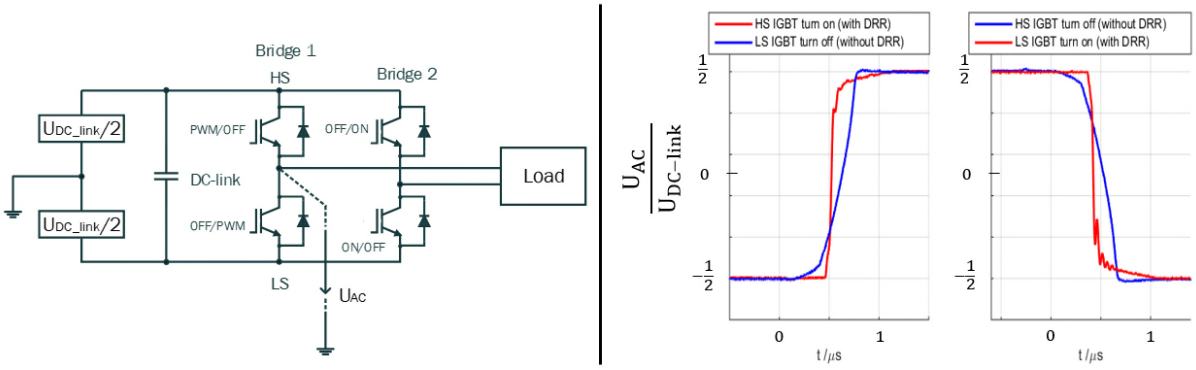


Fig. 3-6: Two types of rising / falling edges on the middle point of a half-bridge (U_{AC}) in power module under low load current (20A)

The mechanism of producing the falling edges of U_{AC} is similar. Taking the falling edges of U_{AC} in Fig. 3-8 and Fig. 3-10 as example, when the LS (low side) switch is off, the HS (high side) diode is conducting the load current (status 4). If the LS switch receives a gate signal and turns on again, the DRR of the HS diode occurs for a short while (status 5) and the load current commutates to the LS switch to flow continuously (status 6). During this transition from status 4 to 6, a steep falling edge is built up between the middle point of the bridge and the ground. The edge turns to be gentler, if the current commutates to the diode turning off the HS IGBT, which is illustrated in Fig. 3-10Fig. 3-9. In status 3, the HS switch is driven by the gate signal and turns off. The load current is forced to flow through the LS diode of the same bridge (status 1) and causes a free-wheeling process. A relatively gentle edge of U_{AC}, compared with the situation in Fig. 3-8, is built up thereby.

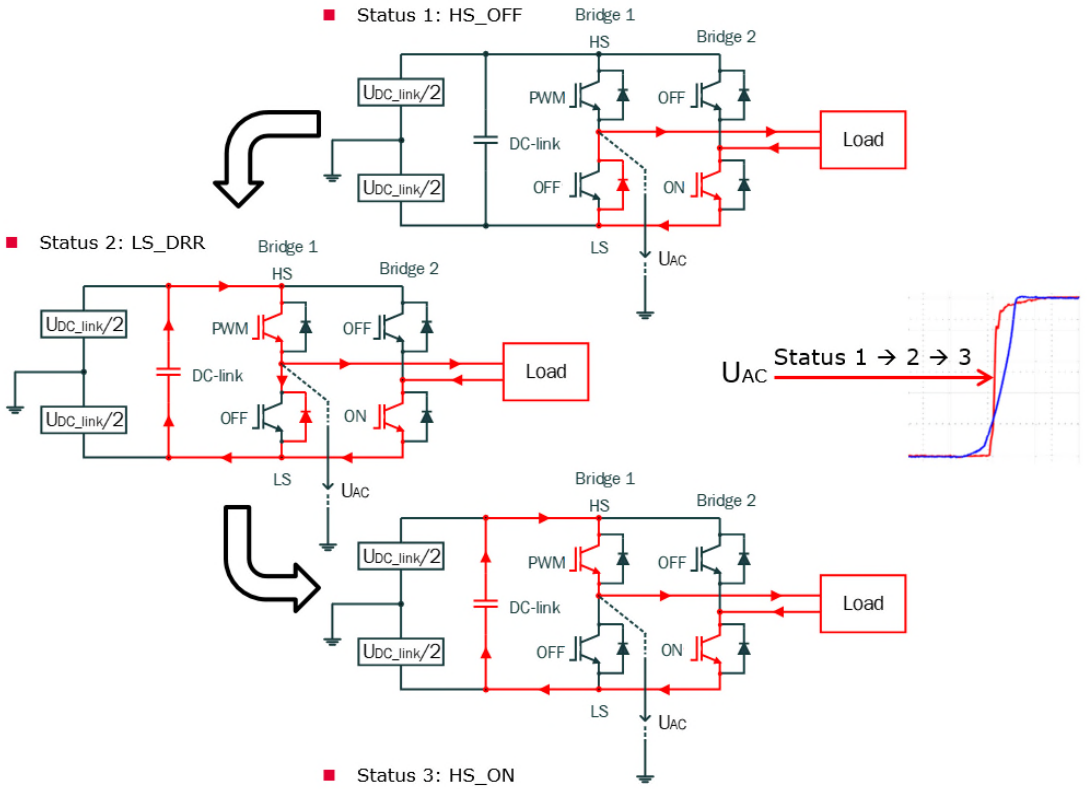


Fig. 3-7: Mechanism of producing rising edge with DRR

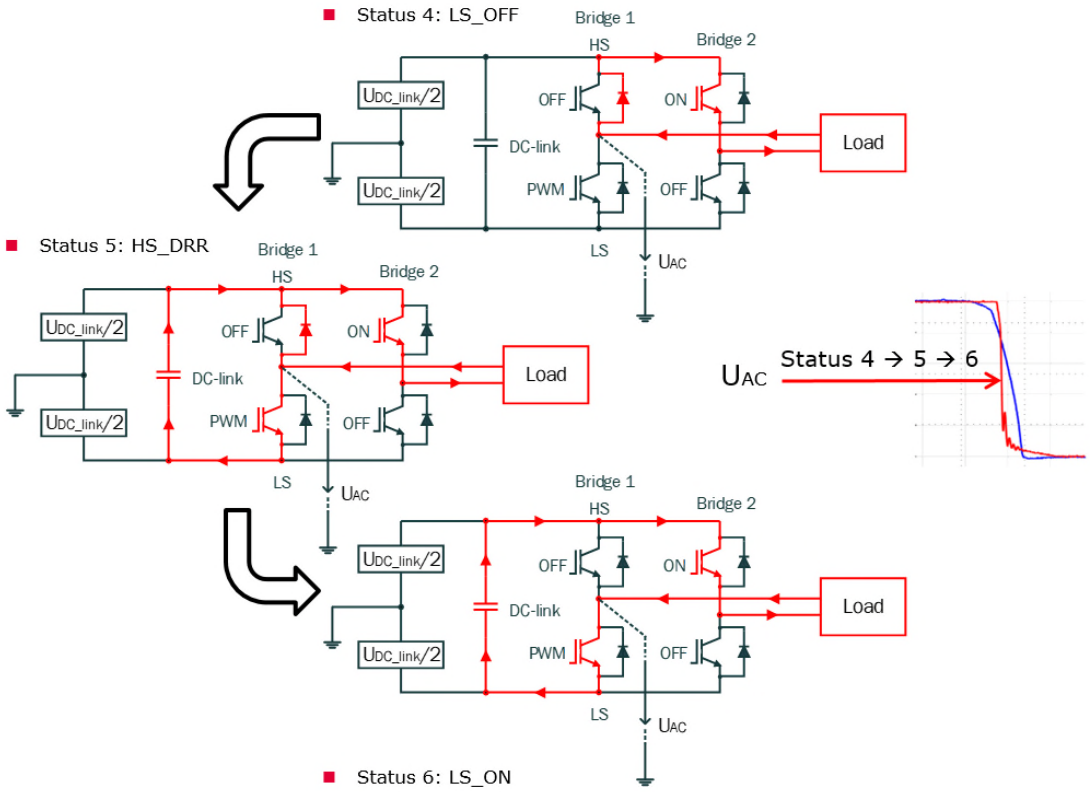


Fig. 3-8: Mechanism of producing falling edge with DRR

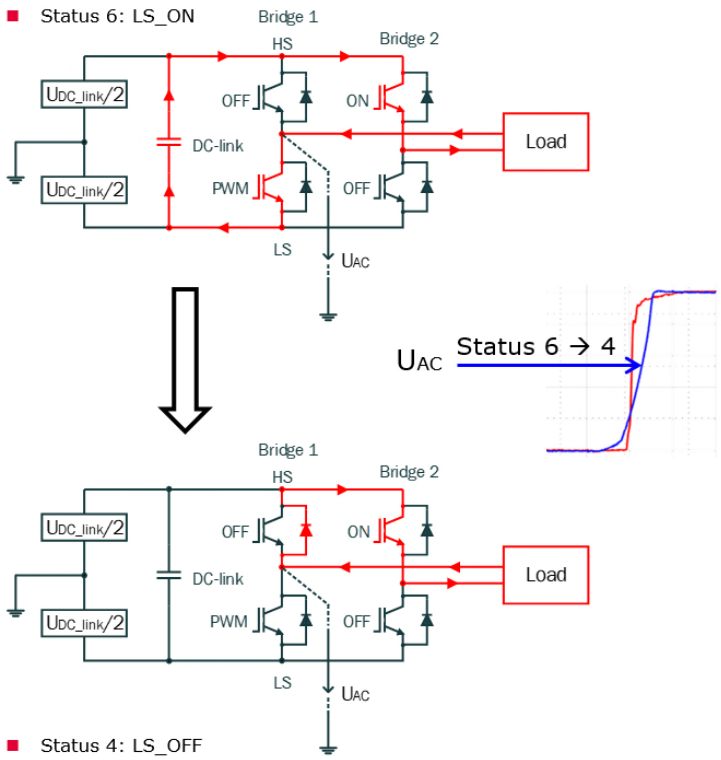


Fig. 3-9: Mechanism of producing rising edge without DRR

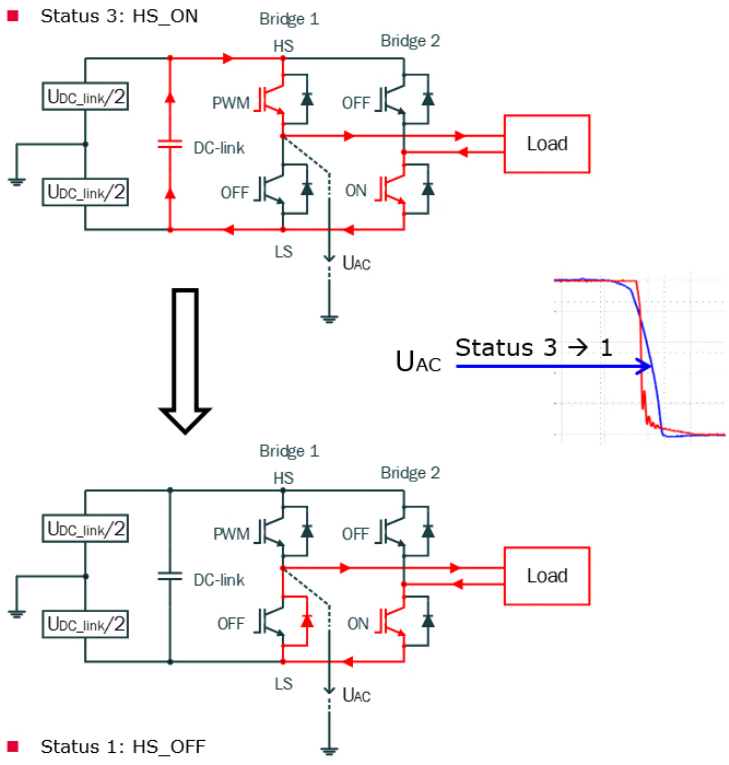


Fig. 3-10: Mechanism of producing falling edge without DRR

3.2.2. Inconstant dv/dt because of variable load currents

As mentioned before, compared to the commutation occurring by starting free-wheeling processes of the diode, the $\mathrm{dv/dt}$ of the rising edges (or falling edges, depending on whether high or low side IGBT is switched) turns out to be significantly higher when the DRR is involved in the commutation. From the EMI point of view, these two types of edges are classified as critical (with high $\mathrm{dv/dt}$) and uncritical (with low $\mathrm{dv/dt}$) in this chapter.

The buck-converter operation always includes one critical edge and one uncritical edge to build up a whole pulse in each switching period: During operation of the HS IGBT, the rising edges are steep (in red) and the falling edges are smooth (in blue); during operation of the LS IGBT it turns out to be the opposite situation. The measurement results in this work confirm that the $\mathrm{dv/dt}$ of the edge is not constant when the load current changes its value. Fig. 3-11 shows that the $\mathrm{dv/dt}$ of the rising edge in U_{AC} under the DRR effects slightly decreases when the load current of the system increases. The voltage curves appear increasingly more “stepped” as the load current increases, the reason for that can be explained through Fig. 3-11: When the HS IGBT is turned on again and the LS diode reversely recovers, the stray inductance of the power module and the DC-link during $\mathrm{di/dt}$ phase constitute a voltage divider of DC link voltage, leading to the observed plateau as well as smoother slope. The length of this plateau increases when the load current increases.

On the other hand, the falling edge becomes increasingly more critical under high current. This is because the voltage peak at the end of the slope, which is caused by the leakage inductance (approx. 20 nH) of the power module and the DC-link during the IGBT turn-off, cannot be neglected anymore when the $\mathrm{di/dt}$ is big enough and the charging current for the output capacity (the parasitic capacitors of the power module and also from the load-side) is higher.

These changing slopes will lead to different EMI spectrums. As shown in Fig. 3-12, the measured rising and falling edges by different load current can be used to build up artificial pulses in time-domain, then FF-transformed to respective spectrums in frequency-domain. Through this procedure it can be seen, that the rising as well as falling edges dominate different frequency areas under different load currents. Therefore, it is not possible to estimate the EMI worst-case if the load current remains unchanged.

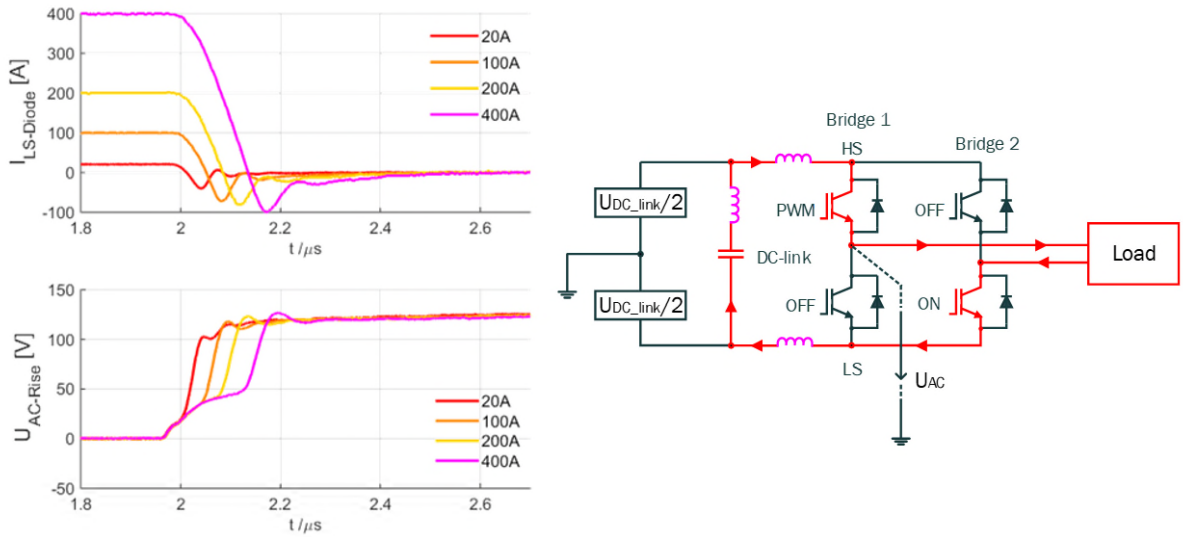


Fig. 3-11: Increased load currents (left top) acting on the stray inductance (approx. 29nH) of the power module and the DC-link (right) lead to "stepped" voltage curves at the middle point of a half-bridge (U_{AC}) (left bottom). Measured at room temperature.

The load current in buck-converter operation is almost constant. In contrast, as summarized in Fig. 3-13, the load current of inverter operation has sinusoidal shape. Within one operation period, the load current consists of one positive half wave and one negative half wave. The positive half period can be considered as the buck-converter operation with the HS IGBT switched on and off; while the negative half period can be seen as it with LS IGBT switched. During each period, the IGBT in buck-converter should switch with variable pulse width so that the amplitude of the load current can keep changing over time. In this case, from EMI point of view, in areas 1 and 3, the turn-on edge dominates because of DRR and then leads to worse EMI performance in high frequency area; in area 2, the turn-off edge dominates because of high $\mathrm{d}i/\mathrm{d}t$ and then leads to higher spectrum in middle frequency area. It can be concluded that the EMI worst-case in inverter operation may differ from EMI in buck-converter operation with fixed current.

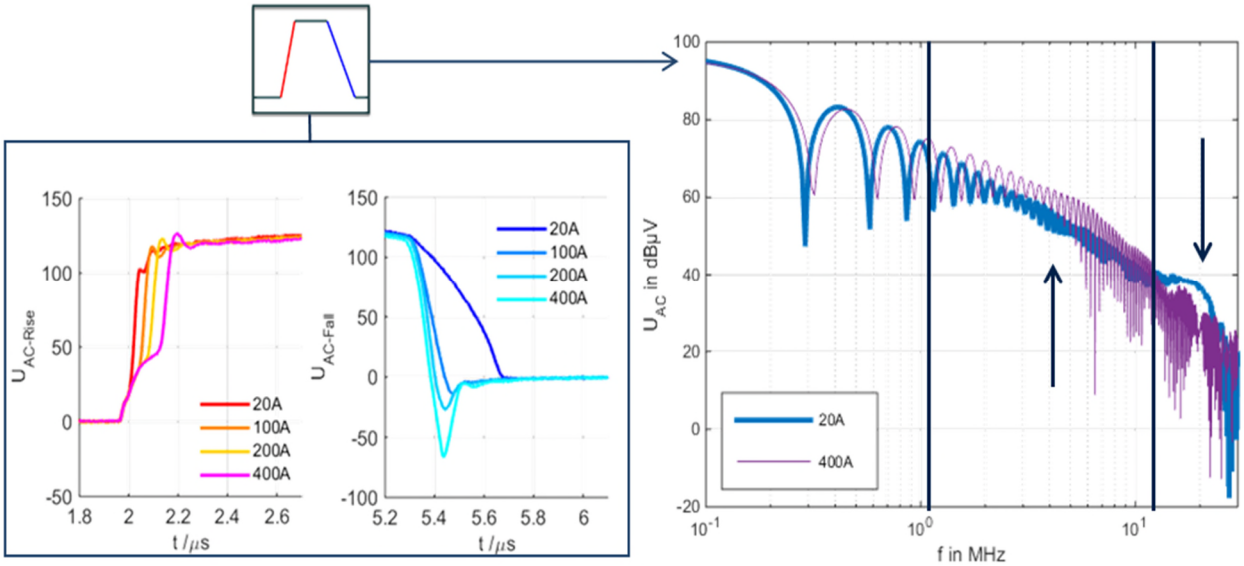


Fig. 3-12: Artificial voltage pulses which are built up from measured rising and falling edges by different load current (left) and their FF-transformed spectrums (right)

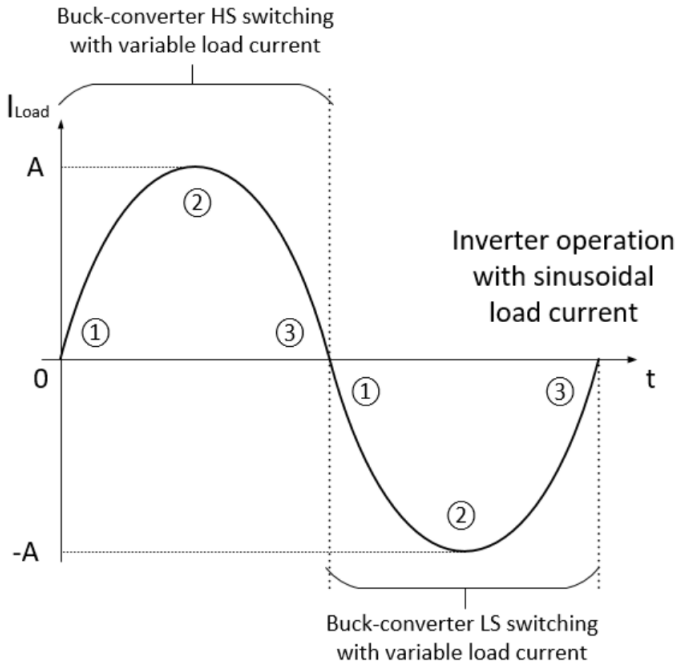


Fig. 3-13: Dividing time areas by comparing the load current of inverter (sinusoidal) and the load currents of buck-converter (constant)

3.3. EMI performance of the SiC diode without DRR effect

As a further step of the work, the behavior of other types of diodes may be of interest. Silicon carbide diode belongs to the wide bandgap semiconductor family. Since there is no need to remove excess minority carriers from the n-region of silicon carbide devices, as in the case of silicon pn diodes, these devices have no reverse recovery current [20]. It has been confirmed in [14] that the EMI performance becomes better when a SiC diode replaces a Si diode being snappy (e.g., with a fall time less than 5 ns at a voltage rating of 1200 V) and having a high amplitude of reverse-recovery-current. It means that if only considering the effect of diode snappiness, it would bring about only little benefits in terms of EMI to replace a less snappy Si diode (e.g., with a fall time more than 20 ns at a voltage rating of 1200 V) with a SiC diode. The significant EMI reduction from 50 MHz and above can be achieved by replacing a snappy diode with a SiC diode by removing the reverse recovery current.

For this dissertation, it is focused on the $\mathrm{dv/dt}$ of the middle point of the half bridge against ground (U_{AC}), being high under low load-current due to DRR effect. This can be expected to change when a SiC Schottky barrier diode would be used which turns off with capacitive behavior and without reverse recovery. The $\mathrm{dv/dt}$ at turn-off and turn-on might then have a similar current dependence. This forecast can be confirmed by the following measurement results: The 650 V SiC Schottky diodes of Infineon®'s 5th generation are integrated in an automotive power module (abb. as "SiC Module"). The module is then compared with the same

type of module equipped with standard diodes (abb. as “Std. Module”) regarding their $\mathrm{dv/dt}$s of the U_{AC}. In Fig. 3-14 left it can be seen that under different load currents (20 A and 400 A, RMS values), the power module with SiC diodes shows generally the same behavior as the module with Si diodes. For the SiC module, the deformation of the rising U_{AC} edges caused by the module stray inductance is still visible. By the falling edges of U_{AC}, the shape of the curves is mainly depending on the turn-off process of the HS IGBT in the half-bridge (see chapter 3.2.1). Since the IGBT of both modules are from the same type, there should be no difference to show by the U_{AC} falling edges under the same load currents. This is confirmed by the measurement results in Fig. 3-14 left bottom.

However, the SiC module can also be easily distinguished by the ripple after U_{AC} rising edges in Fig. 3-14 upper left. It can be concluded, that the SiC diodes cause oscillation during the turn-off process. As a further step of the research, the switching moments of both power modules are recorded and presented in Fig. 3-15. In the measurement, the HS IGBTs of the modules are turned on to commutate the load current from the LS diodes (see Fig. 3-7 in chapter 3.2.1). At the same time, the SiC diode acts much more “unsmooth” than the Si diode. There is no more reverse recovery current to see, yet a ripple of swinging sinusoidal wave is added to the diode turn-off current. The origin of the ripple seen after U_{AC} rising edges at the SiC module can be explained as follows: The turn-off current of the SiC diodes with extremely high $\mathrm{di/dt}$ is caused by removing its electrons, which are the only charge carriers in its unipolar structure. Since the SiC material has much higher dielectric breakdown field (usually 2 to 3 MV/cm, approx. 10 times that of Si), the SiC schottky diode is usually produced with much thinner structure than the normal Si PN diode of the same voltage class (in this work 650 V). This thinner structure leads then to larger capacitance of each chip. The typical capacitance of the used SiC diode in this work, according to Infineon® datasheet, is 76 pF (measured at V_R=300 V, f=1 MHz) per chip. The total capacitance of each switch, which consists of 32 SiC diode chips (each chip for 20 A rating current), is then 2.43 nF. This capacitance will combine with the stray inductance of the power module and the DC-link (overall approx. 29 nH, see Fig. 3-11) to cause an oscillation with the frequency of approximately 20 MHz in the commutation cell.

To predict the differences between Si and SiC diodes regarding their EMI behaviors, the same procedure for signal processing shown in Fig. 3-12 is used again to build up artificial pulses in order to execute the FF-transformation. The measured rising as well as falling edges in Fig. 3-14 left side are transformed into the spectrums in Fig. 3-14 right side. The aforementioned ripple caused by the SiC diode in the U_{AC} rising edges is transformed to an obvious peak at approximately 20 MHz in the spectrum of the SiC module. The amplitude of the peak turns out to increase when the load current is larger (from 20 A to 400 A). Generally, the SiC module always shows higher EMI (in 100 kHz to 30 MHz area) than the Std. module because of this extra peak in the spectrums.

To confirm the existence of the 20 MHz peak caused by the SiC diode, the conventional EMI measurements based on the standard for automotive application [67] are subsequently carried out. The results are presented in Fig. 3-16. It can be seen that in the frequency domain until 300 MHz, the power module with Si- and SiC-diodes generally show matched spectrums to each other. The extra peak at about 20 MHz caused by the SiC diode is still visible and therefore leads to worse EMI behavior in this frequency area.

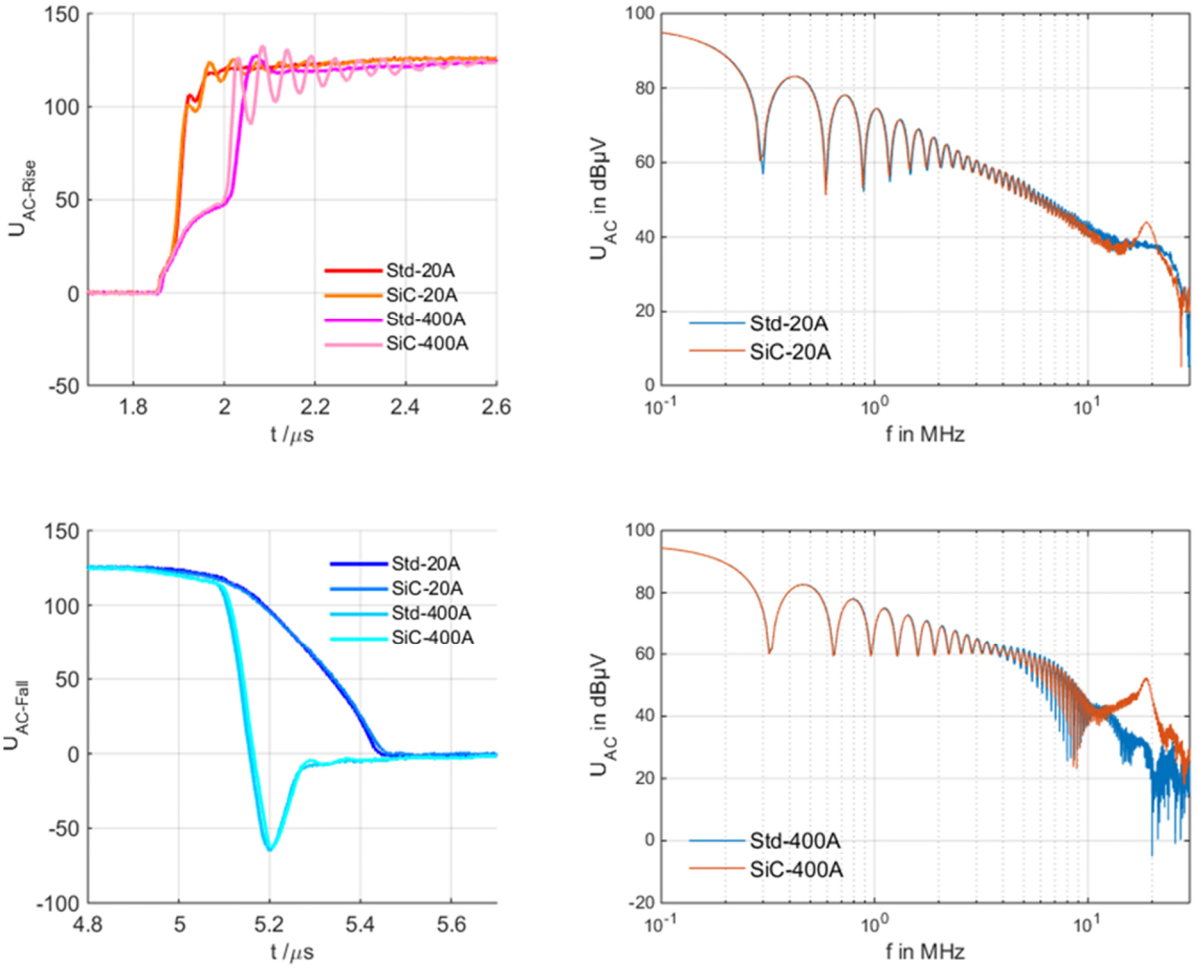


Fig. 3-14: Comparison of the U_{AC} rising and falling edges between Std and SiC module (left) as well as their FF-transformed spectrums (right) under different load currents

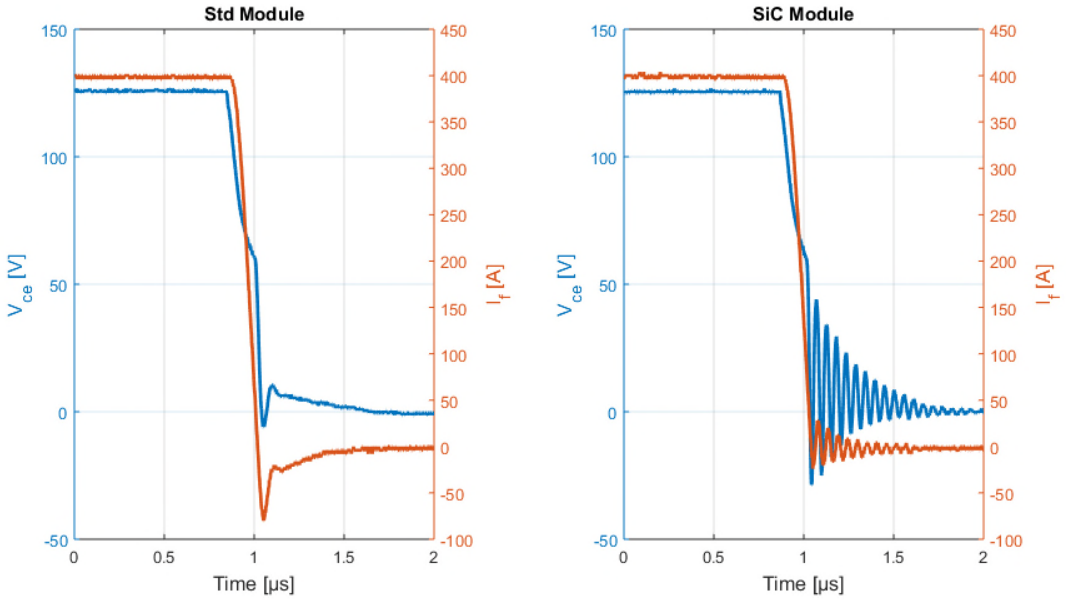


Fig. 3-15: Comparison of the switching behavior of the power module with Si diode (left) and with SiC diode (right): The collector-emitter-voltage (blue) on the LS IGBTs, as well as the current through the HS diodes (orange)

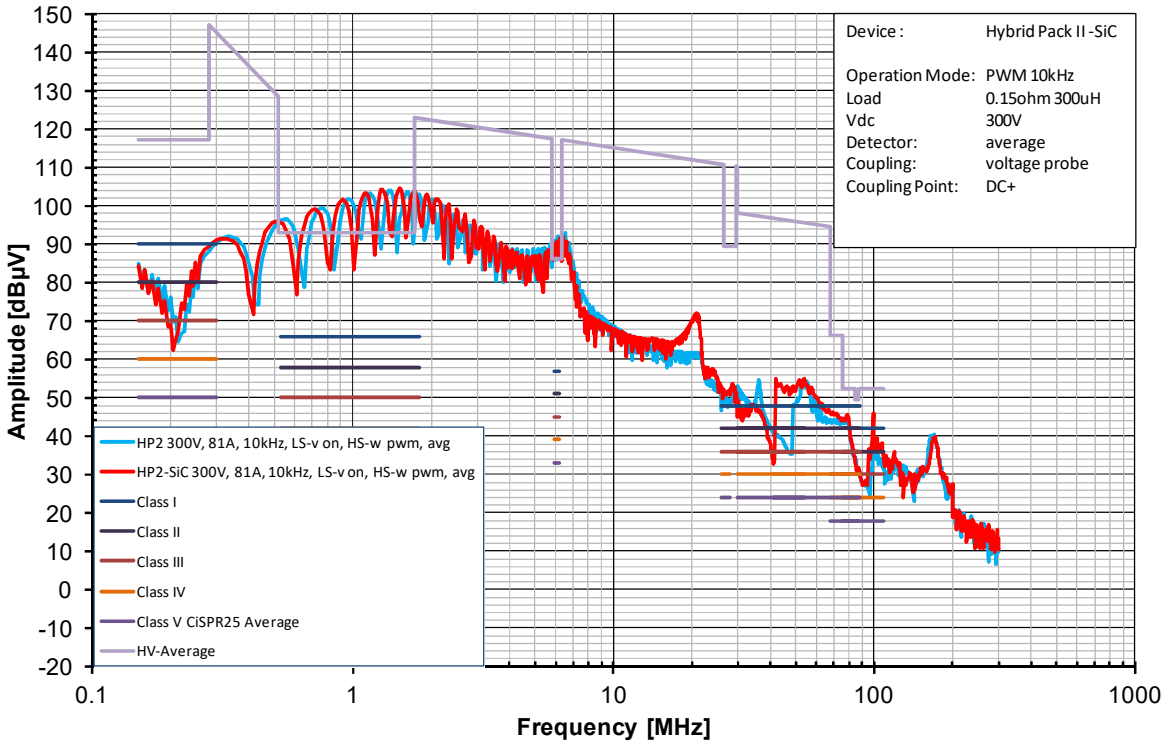


Fig. 3-16: Confirmation of the existing of the extra peak in the spectrum caused by usage of SiC diode by carrying out the conventional EMI measurements

4. Analysis of power module's EMI performance on system level

In the previous chapter, the switching edges, respectively the high frequency pulses which are generated during the operation of the power semiconductors, are investigated. Because they are considered as the main source of the conducted and radiated EMI, to facilitate our understanding of the effects, the relevant mathematical calculations are carried out, together with the interference mechanism analysis and the measurement verifications.

As a further step, based on the understanding and the conclusions from the previous chapter, the discussion will stretch into the level of the drive system in the automotive application. Obviously, there is no point in investigating the characteristics of the interference sources without considering the other existing components in its application environment. For a general automotive application system, the wideband conducted EMI can be amplified or reduced in different frequency ranges during its propagation, depending on the resonant characters of the other system components, especially their parasitic capacitances and the stray inductances. Certain resonance spots with remarkable amplitudes are usually caused by certain current loops comprising different LC components in the drive system [40][41], such as the LISN components, the stray inductances of the HV wires and the DC-link as well as its busbar [19], the parasitic capacitances of the motor windings and the power module, etc.

In order to improve the power module's EMI performance, there is a necessity in the first place to clarify and evaluate its current status. To achieve this goal, the setup and test bench of the conventional EMI measurement for the typical automotive application are firstly presented, as well as the measurement approaches used in this dissertation being explained. Next, the simplified time-domain simulation models in system-level are presented and verified. Through the simulation, the influences stemming from the power module to the system can be better elucidated; the importance of different factors inside / outside of the power module can be therefore evaluated. Furthermore, the simulation models can also be used to predict the EMI performance, if some of the parameters in the system are intentionally changed.

4.1. Conventional EMI measurement methods for automotive drive system

For the power module manufacturer, to evaluate the actual state of the products and to make improvements regarding the EMI performance, always indispensable is a test bench, which makes possible the EMI measurement of the power module without being disturbed by other interference sources. Hence, the test bench used in this dissertation, which is built up

according to the conventional requirements for the EMI measurement in the automotive application, shall be introduced.

A complete EMI measurement according to CISPR-25 [67] includes both conducted and radiated interference measurements. The conducted interference is measured at a LISN (see Fig. 2-10) in relevant frequency range according to the standard, while the radiated interference is measured with an antenna in higher frequency range. In the current state of the art, for the use of IGBT inverters in the electrical and hybrid vehicles' drive systems, the electrical drive train shall be completely electrically shielded to reduce the radiated emissions. Since this work focuses on the conducted interference, the test bench used in this dissertation only enables measurements on the conducted emissions of an unshielded system. The reason for choosing the unshielded test setup is that it can reduce the system complexity and focus more on the power module itself. Certainly, the question emerges: What will happen when (as it is in the real application) shielded cables are used? Regarding this question, a parameterizable chain conductor model of a coaxial cable has been created and thus a simulative comparison is carried out in [82]. By comparing with the shielded case, Spanos and Keller concluded, that the unshielded system shows "slight reduction of the broadband emission above 10 MHz", as well as "shifting of the resonances of the system to lower frequencies in particular." The reason lies in the parasitic components of the two cable types: "Although the shielded cables have a higher parasitic capacitance to ground (which would cause a reduction in the resonance frequencies), but since the inductance of coaxial shielded cables is much lower, an overall increase of the resonance frequency is caused." For the experimental approaches in this dissertation, the standard limits are not specially taken into account, since the focus of the work is investigating and analyzing the EMI matters, instead of complying with the standards.

4.1.1. Measurement approaches with LISN

One of the popular EMI measurement methods is measuring the conducted emission voltage drop (in dBµV) through the device LISN (Line Impedance Stabilization Network). The principle of the measurement setup is shown in Fig. 4-1. Connected to the HV battery, there is usually a LISN in the HV+ and another in the HV- wire. Through the receivers in the LISN, the conducted emissions that flow in the HV system can be measured. In order to reproduce the coupling effects between the HV system and the grounding of the car chassis, corresponding to the CISPR-25 [67], the measured object is located at a distance of 5 cm above a metal surface. The HV system is therefore galvanically insulated from the grounding surface. The LISN for high voltage systems distinguishes itself from the LISN for low voltage systems only in the input capacitor. The input capacitor of the HV-LISN is 1 µF according to the current version of the CISPR-25 Ed. 4. In the experiments of this dissertation, in order to avoid the circumstance that the isolation monitor of the test bench is activated, the input capacitor of the HV-LISN is reduced to 100 nF. This will lead to the shifting of a resonance point from low frequency range to higher frequency area; however, the principle of the conducted EMI measurement remains unaffected.

Generally, the power supply for controlling the tested power module is implemented with a DC-DC converter in the fly-back structure. With a supply voltage of 32 V, the DC-DC converter is

operated at the switching frequency of 300 kHz. For every half-bridge of the power module, one transformer for controlling is used for the supply of the HS IGBTs and one for the LS IGBTs. In a special test, batteries are used as the supply for the IGBTs' driving signals in order to investigate the influence of the DC-DC converters on the EMI measurement result. Thereby the DC-DC converters can stop working, thus spreading no longer extra interferences into the measured HV system. The measurement results are shown in Fig. 4-2. The two blue curves show the conducted EMI on the HV- wire with full operation of the inverter, i.e., the HV voltage is applied and the IGBTs are switched. In dark blue, the measurement is done with active DC-DC converters, while in light blue with battery replacement. The violet and the green curves show the interferences by the status, in which the IGBTs are being switched, without the HV voltage is supplied. In this case, the violet curve shows only the interferences from the driving signals of the IGBTs because of the use of the battery as power supply, while the green curve shows additional interferences from the DC-DC converter.

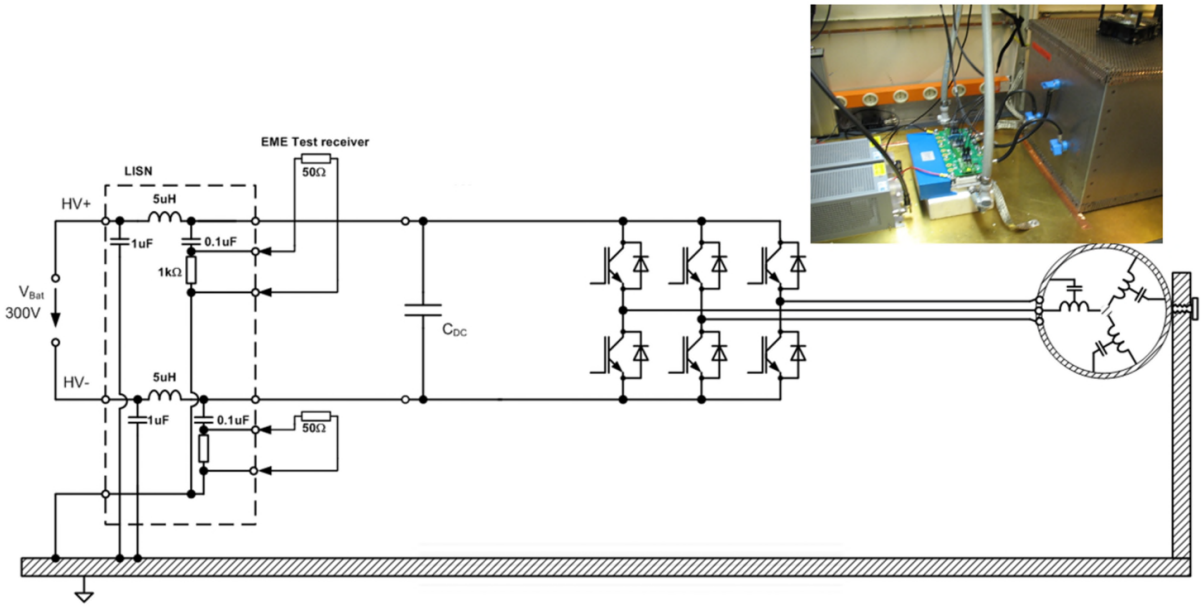


Fig. 4-1: Test bench based on the conventional EMI measurement principle (from left to right: LISN, DC-link, power module, "load box")

While the increase of emissions caused by the DC-DC converter can be easily recognized by comparing the violet and the green curves, the amplitudes of two blue curves are almost identical, which means, the DC-DC converter has almost no influence on the measurement results by the HV wire. It can be further concluded that the conducted interferences measured in the presented setup by the HV wire originate only in the switching IGBTs.

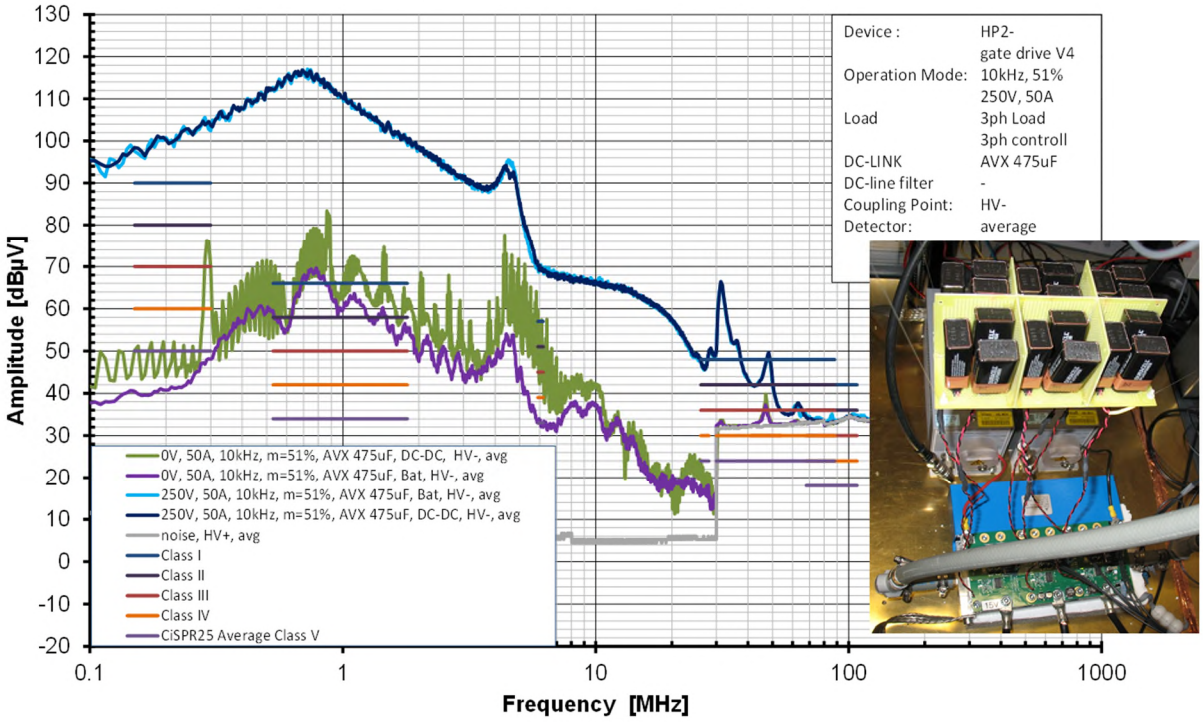


Fig. 4-2: Deactivated DC-DC supply via batteries (bottom right) and EMI evaluation of the DC-DC converter, i.e., f_{switch}=10kHz, dark blue and light blue: active inverter, V_{DC}=250V; Green: DC-DC converter as supply, V_{DC}=0V; Violet: battery as supply, V_{DC}=0V

4.1.2. Measurement approaches with current sensor

In the case of the approaches with LISNs in the HV system, the measurement positions of the conducted EMI are at the HV+ or HV- battery wires. For a verification of the propagation paths of the interferences within the system, it is significant to measure the currents on various connecting positions within the electrical drive train by a HF current clamp. Therefore, the common-mode currents are measured on the AC cables (U-V-W) as well as on the two ground straps of the power module and the "load box" (assigned by Bosch). The load box serves as a reproduction of the electrical parameters of the motor, which are relevant to the EMI measurement. Fig. 4-3 shows the positions of the current clamps used for the approaches in this part. Fig. 4-4 shows the results for those different measurement positions accordingly.

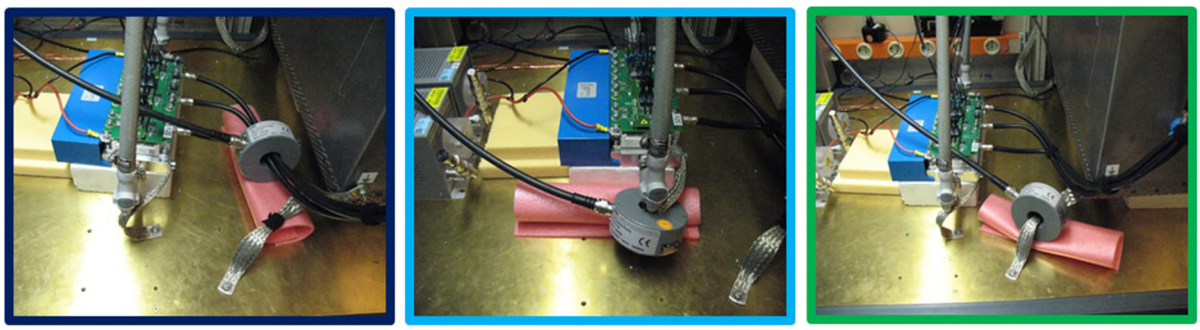


Fig. 4-3: Measurement of the common-mode interference currents: HF current clamp on the AC cables (left); on the ground straps of the power electronics (medium) and the load box (right)

The green curve shows the common-mode current flowing between the load box and the grounding caused by the dv/dt of the installed capacitors between the inductive coils and their housing. The capacitors are located in the load box to reproduce the parasitic capacitances of the motor windings. This current is created originally by the switching IGBTs. Should there be no alternative paths available for this current to flow back to its sources, i.e. the IGBTs, it would close the loop by flowing via the capacitances of 0.1 µF in the LISNs which lie in between the DC-link wires and the grounding surface of the test bench. This current is then visible in the conducted EMI measurements. On the other hand, since the IGBTs (and diodes) also have parasitic capacitances to ground via the module substrate and heat-sink, common-mode current is also present in the ground strap of the power electronics (light blue curve). Regarding this issue, further detailed discussions and investigations can be found in chapter 5.1.2 and 6.1.1.

The dark blue curve shows the common-mode current of the AC cables. From the curves it can be seen that the amplitude of this current is identical to the current flowing between the load box and the grounding. The common-mode current of the load box flows therefore fully through its ground strap. From the aspect of the drive system, these measurement results are also good exemplifications to show that the grounding concept of the power module as well as the electrical motor shall be considered as one of the essential topics for conducted EMI research.

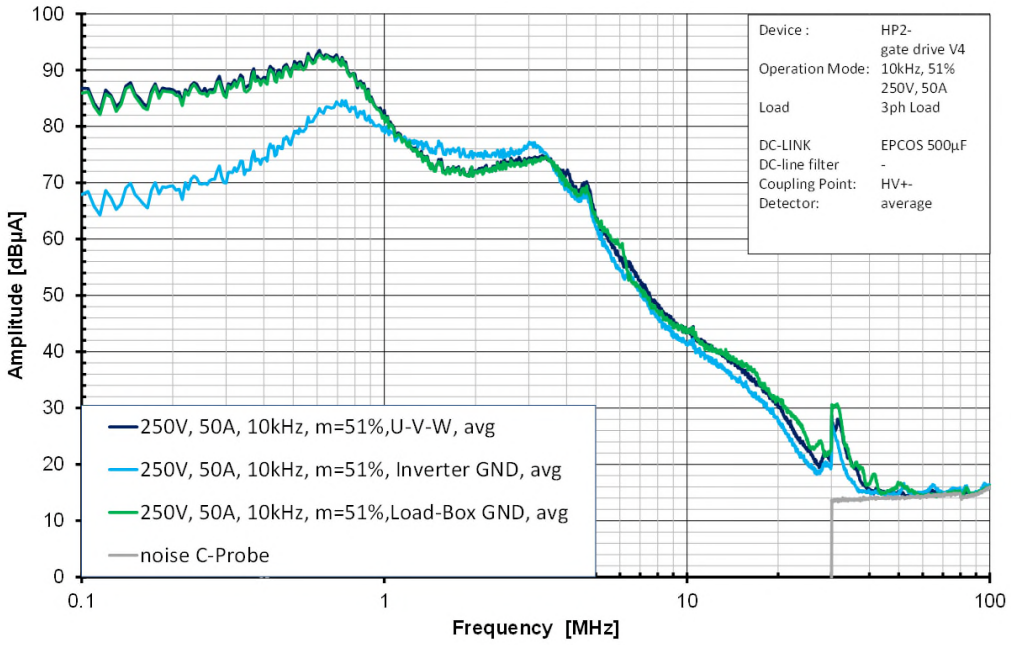


Fig. 4-4: Conducted EMI measurement results of the approaches with the HF current clamp

4.2. Time-domain simulation models for conducted EMI analysis

The building of the simulation models serves to understand the mechanism of how the conducted EMI noises originate and spread in diverse levels of the system [22][40][78]. The conclusions about the EMI behavior with regard to different interference modes can be achieved through the simulation. In this dissertation, the main purpose of simulation is to use the simulated results to investigate the principles of the interference propagation. Most measures for EMI reduction and their evaluations (except for the X-capacitors' impact on the DM interferences), are not demonstrated from the aspect of simulation. Instead they will be extensively discussed in chapter 6.

4.2.1. Simplified time-domain simulation with separated common- and differential-modes

The preferred simulation models to be discussed at first are based on Hoene's model in [2]. According to the various manners of the EMI propagation (common mode and differential mode), the interference source is divided into two parts. The changing current in the DC-link is considered as an interference source of differential mode and can then be modeled by an equivalent, idealized current source. The trapezoidal changing potential at the output node of the half-bridge (also called AC node, see chapter 3.2) is considered as a common mode interference source and can be modeled by an equivalent, idealized voltage source.

The simulation model of the common mode is shown in Fig. 4-5. The components of the whole system are marked with different blocks (e.g. LISN, battery cables, DC-link, load and parasitic capacitance against GND, etc.). The voltage source at the output node of the half-bridge feeds a series of trapezoidal pulses into the system. The steepness of the pulses' edges is determined according to the measured turn-on and turn-off times of the power semiconductors. While measuring the HS IGBT turn-on process, it takes approx. 100 ns until the voltage at the AC node rises from 0 to 125 V. In the opposite direction it takes twice as long, if the IGBT switches off again. The battery and motor cables, which are used in the setup in 4.1, can be modeled by inductances. The values of the inductances are determined by calculation on the basis of the formula presented in [5]:

$$L_p = \frac{\mu l}{2\pi}\left[\ln\left(\frac{l}{r_0}+\sqrt{\frac{l^2}{r_0^2}+1}\right)+\frac{r_0}{l}-\sqrt{\frac{r_0^2}{l^2}+1}\right] \qquad \textbf{(4-1)}$$

The formula is suitable for the calculation of the partial inductance of a cylindrical wire. Where l is the length and r_0 is the radius of the wire. The partial self-inductance of round conductors (including the internal inductance) can be easily determined by adding the radius-independent value of 50 nH per meter to the external inductance [5]. In this dissertation, the motor cable is also estimated in this way, without consideration of the mutual inductances. To make the simulation work, the negative pole of the interference voltage source must be connected with

a very large resistance of 10 GΩ and thus grounded. The inductances between DC-link and voltage source represent the bonding wires and conductor tracks, which connect the semiconductors' chip metallization and the power module screw connections. Usually, the DC-link capacitor plays no role in the common mode simulation model [71]. However, with respect to HV+ and HV-sides, differences and unbalances of the system components are unavoidable. For that reason, the DC-link capacitor can influence the common mode interference paths as well. The coupling capacity of the power module against the reference ground is quantified by a 3D extraction from the design data of the module. This part describes the parasitic capacitive connection between the collector of the LS IGBT (identical to the emitter of the HS IGBT) in the half-bridge and the bottom side of the DCB, which is connected directly to the heat-sink of the power module.

The course of the simulation signal in time domain is detected via the voltage drop at a 50 Ω resistor in the LISN, then processed by FFT and converted into the spectrum. If one of the parameters of the simulation model is changed, while the values of the other parameters remain constant, then the partial shifting of the spectrum depending on the frequency ranges can be observed (see Fig. 4-6). The entire spectrum can be divided into 4 areas. Each area is mainly affected by one or two components of the system:

- The "first range" begins at 10 kHz (switching frequency of the inverter) and ends at 100 kHz. The spectrum in this frequency band is mainly influenced by the capacity of 1 µF in the LISN. If this capacity is replaced by one of 0.1 µF, an increase of the spectrum amplitude in this frequency range, as well as the shift of the resonance point to higher frequencies, is caused. However, in the EMI measurement, the conducted interferences with the frequency band from 9 kHz to 150 kHz are usually measured by the current sensor connected to a receiver instead of using the HV LISN [67], since the LISN with an inductance of 5 µH is not suitable for this frequency range.
- In this dissertation, the reproduction of the parasitic capacitances of the motor cable against ground, as well as the coupling capacities between motor winding and its housing, is realized by mounting the discrete capacitors of 3 x 2.2 nF into the "load box" (see 4.1.2). These capacitances of the load side influence the "second range" of the spectrum, respectively the range from 100 kHz to about 1 MHz. Minimizing these capacities brings about an obvious attenuation of the interferences.
- The stray inductance of the motor cable influences the magnitude of the spectrum in the "third range" from 1 MHz to about 10 MHz. Large inductance of the motor cable can bring attenuation of the interferences in this frequency area.
- In the "fourth range" from 10 MHz to 200 MHz, it can be seen that both the faster switching speed of the semiconductor and the larger coupling capacitance of the HS emitter to the ground cause higher emissions.

The sensitivity analysis on the influence of the various parameters to the disturbance spectrum shows, this simplified CM model enables a reproduction of the system on a quantitative level. It is important to notice that the inductance of the motor cable must not be neglected in this model; otherwise, the impact of the power module's parasitic capacitance cannot be properly sorted out and observed in the simulation results.

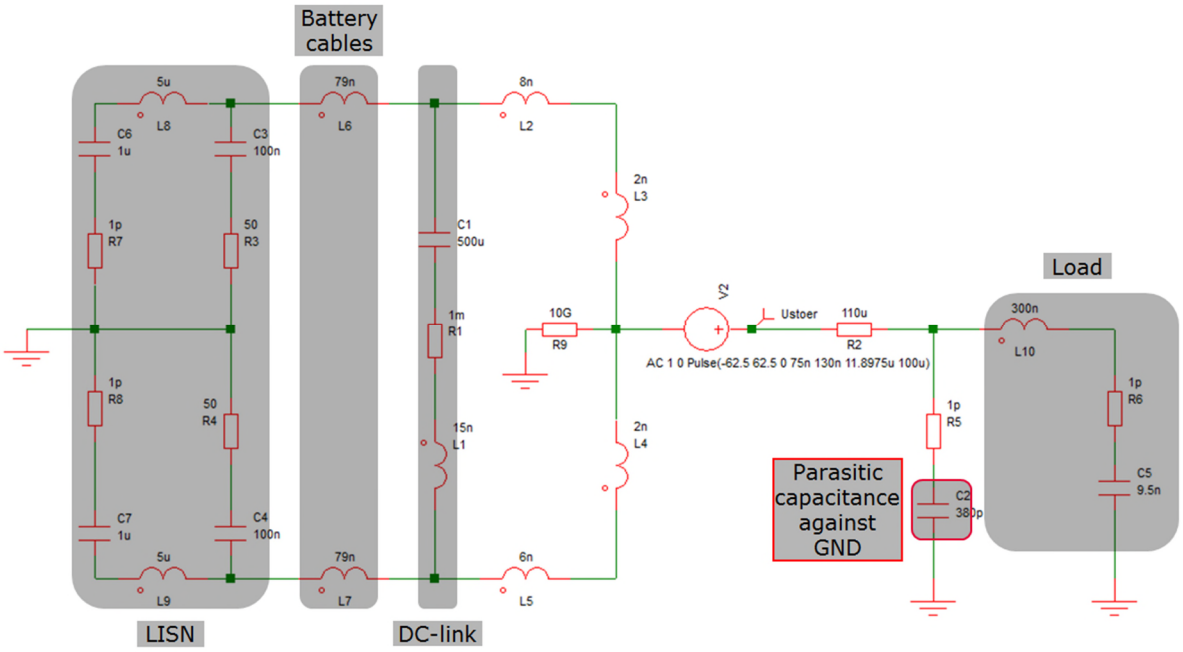


Fig. 4-5: Simplified simulation model for common mode interference

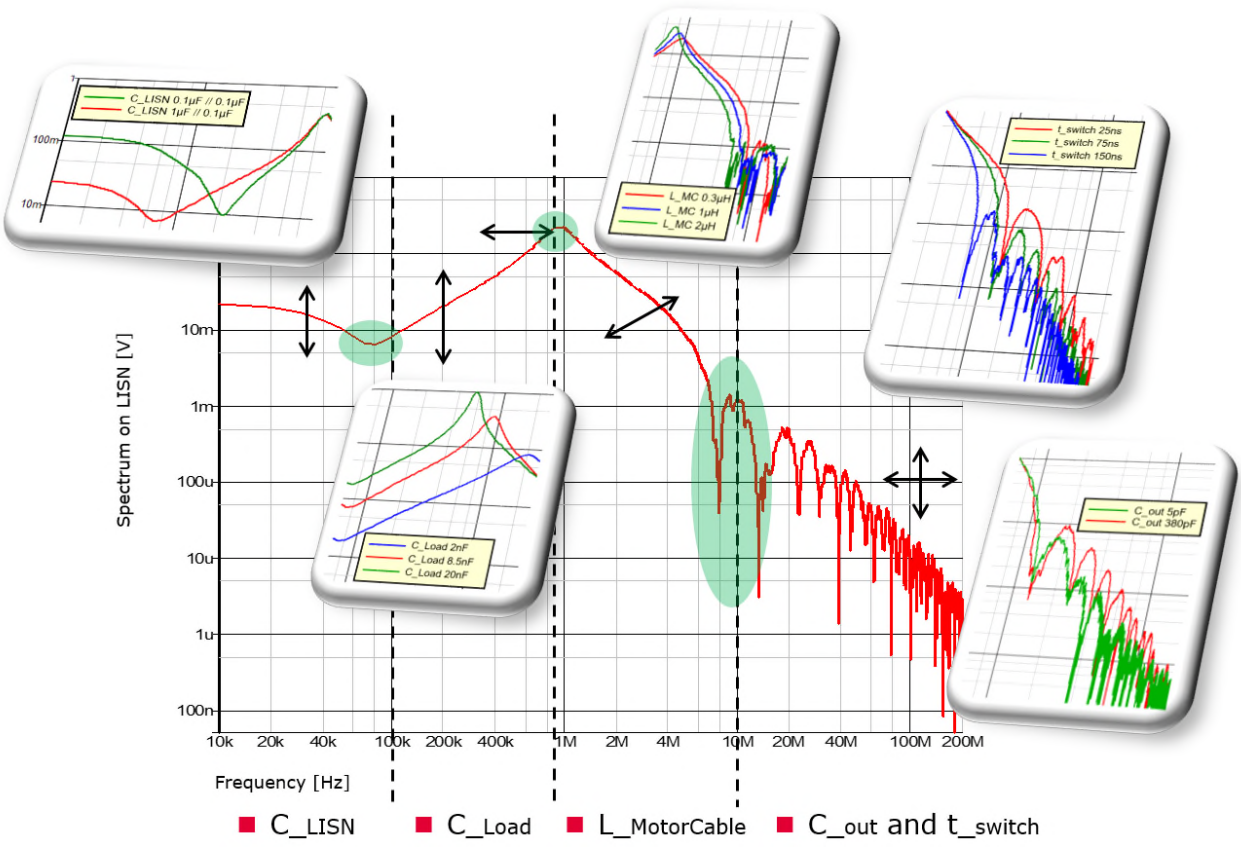


Fig. 4-6: Influence of different system parameters on the CM interference spectrum

In [2], the current variation from the DC-link is modeled by an equivalent, ideal current source. Each time the commutation in the half-bridge occurs, the interference current in differential mode appears. That causes the voltage fluctuations of the DC-link. In this work, these voltage fluctuations in the DC-link caused by the IGBT switching are used as a differential-mode

interference source (see Fig. 4-8 left) for the simulation. The reason why using that to replace an ideal current source can be explained as follows: The periodical ON an OFF switching of the IGBT as well the commutation of the load current lead to the charging and discharging of the DC-link. During these periods, the fluctuating DC-link voltage can be directly measured. The measured data can then be processed and input into the simulation system to play the role as a DM interference source. If an ideal current source were used here instead, it would not be possible to produce enough details of the interference itself. For example, it can be seen in the measured curve that the switching-on process of the semiconductor causes stronger fluctuations in DC-link than the switching-off process does. Such kind of information will be lost when using an ideal current source.

The DM interference source of the simulation model in this dissertation is established as follows:

1) Measuring the voltage drops at HV+ / - against the grounded substrate of the power module during the IGBTs switching-on and switching-off processes (through double-pulse measurement [55] and oscilloscope with the setup introduced in 2.2.2);
2) Processing the measurement data in MATLAB (e.g. normalization of the amplitude, setting of the offset and the pulse width, generation of a continuous signal in a period, etc.);
3) Import the processed signals into the simulation tool SIMetrix via a *.txt file.

The simulation model for the investigation of the differential-mode interferences is shown in Fig. 4-7. In this model, all components are set to be "potential free", that is, there are no galvanic connections from the system to the ground. However, to make sure the simulation in time domain runs, grounding points must be integrated. For this purpose, some resistors with high resistance values (100 GΩ for R1 and R2 in Fig. 4-7) are inserted between the ground and the system in order to keep the system running in an "isolated" state against the ground potential. It is thus possible to view the performance of the DM interference in different frequency ranges.

Comparing the CM spectrum in Fig. 4-6 and the DM spectrum in Fig. 4-8 with each other, it can be seen that the CM interferences dominate in most frequency ranges. Thus, the EMI optimization measures against the CM interferences shall be more effective. The tendency of the DM spectrum is difficult to evaluate above 40 MHz, since excessive noise interferes with the measured signals. If these signals are imported into the simulation and transformed as a source of interference by FFT, the spectrum will thus lose its validity for the reproduction of the conducted EMI in this range.

Besides, the simplified DM simulation model can be used to check the properties and the effects of the X-capacitors as well. It can be concluded from Fig. 4-8 right, that the use of the capacitors results in an attenuation of 6 to 10 dBµV in the frequency range from 2 to 20 MHz, depending on their electrical properties, e.g. the ESL and ESR of the capacitor. On the other hand, new resonances can be built up by the series connection of the inserted capacitor and the stray inductances coming from the power module. However, the new peaks in the DM spectrum caused by the resonances can be covered by the dominating CM interferences in the certain frequency area and ultimately turn out to be invisible in the mixed-mode spectrum.

These conclusions above based on the simulation results shall be verified in chapter 6 and further discussed specifically in 6.2 for more details.

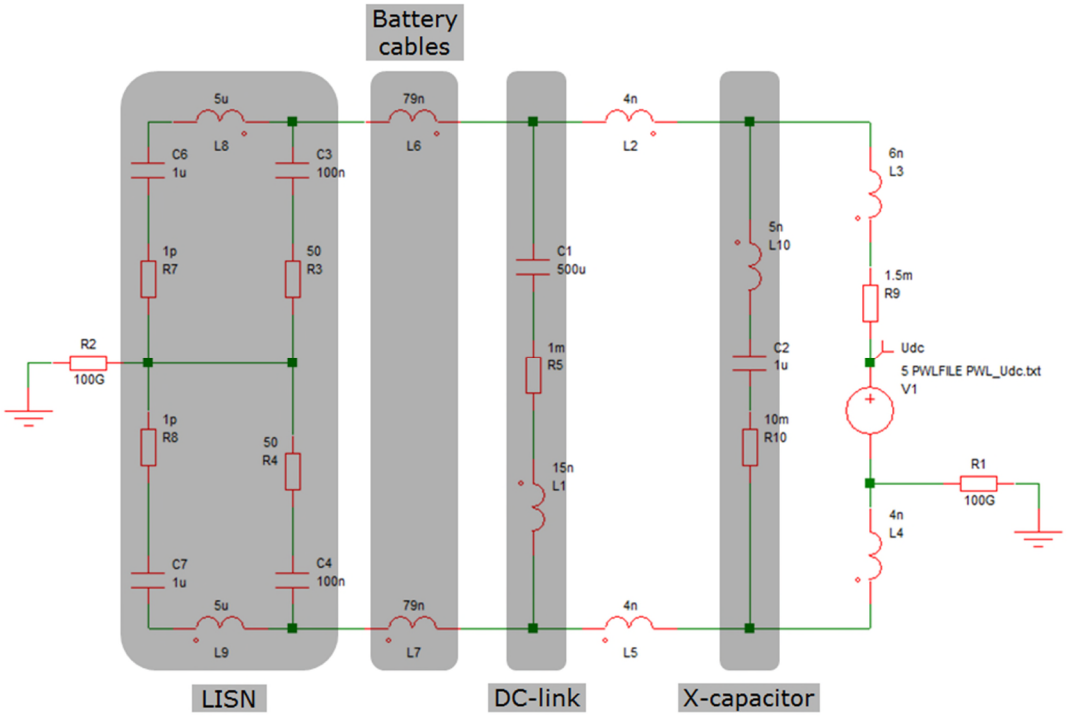


Fig. 4-7: Simplified simulation model for differential mode interference

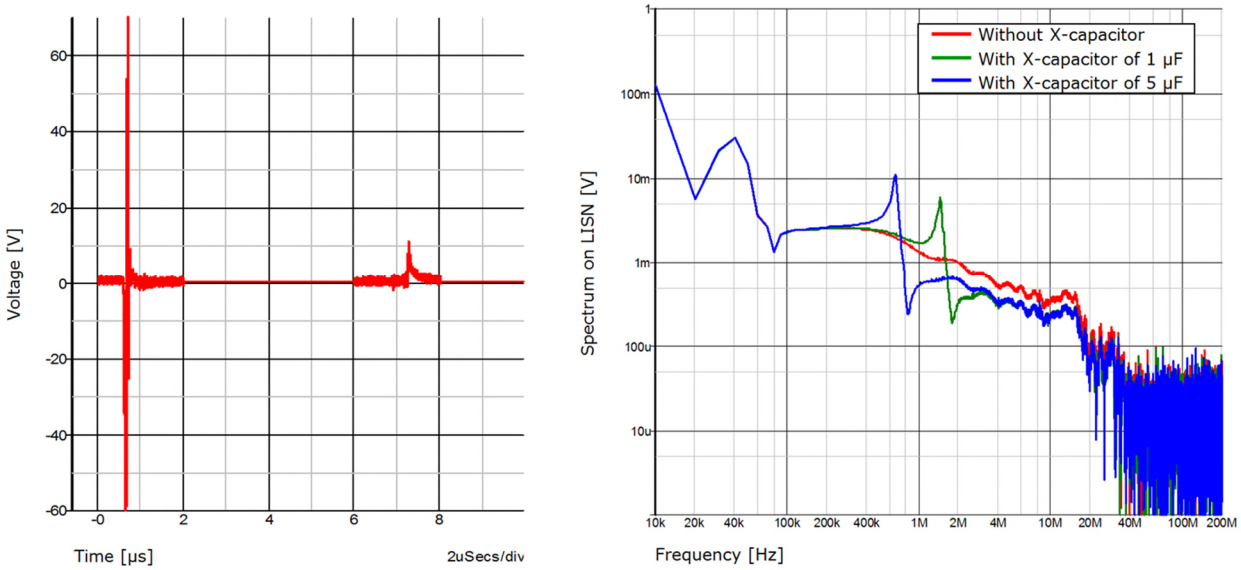


Fig. 4-8: Left: Measured voltage fluctuation U_{DC} in the DC-link, which is used as a DM interference signal in the simulation and right: Spectrum of DM interference, without (red) / with (green and blue) use of the X-capacitors

4.2.2. Refined time-domain simulation for conducted EMI and its verification

Based on the aforementioned separate common- and differential-mode models, the research was expanded on a much more refined model, in which the existing semiconductor models are

integrated to reproduce the "real" interference sources, so that the conducted EMI in mixed-mode (CM + DM) can be simulated and investigated.

In the refined simulation model, the Infineon chip models of 200 A type (the IGBT: *SIGC100T65R3EA_L2*, as well as the diode: *SIDC50D65C8A_XL2*) are used instead of the ideal voltage source in the above-mentioned simplified CM model. Through these chip models the switching processes of the semiconductors can be reproduced by the fundamental trapezoidal pulses with oscillations or over-voltage peaks, which are very similar to the switching behaviors in the real application.

The single-phase buck-converter operation of the power modules was simulated by the refined simulation model in Fig. 4-9. The parasitic components of the system were mainly taken over from the simplified simulation models in 4.2.1, but refined with more details by special consideration of the power module. The parameters are previously determined by calculation or VNA measurements. The examples for the parameterization can be found in 5.1 and 6.1.1. The use of the chip models brings about relatively real switching curves in the time-domain simulation (Fig. 4-10), quite similar to those captured forms during the measurement: For example, the miller-plateau in the gate signal (red), the diode reverse recovery current (yellow), and the overvoltage peak when the IGBT is turned off (blue) etc. can be reproduced and recognized in the simulation.

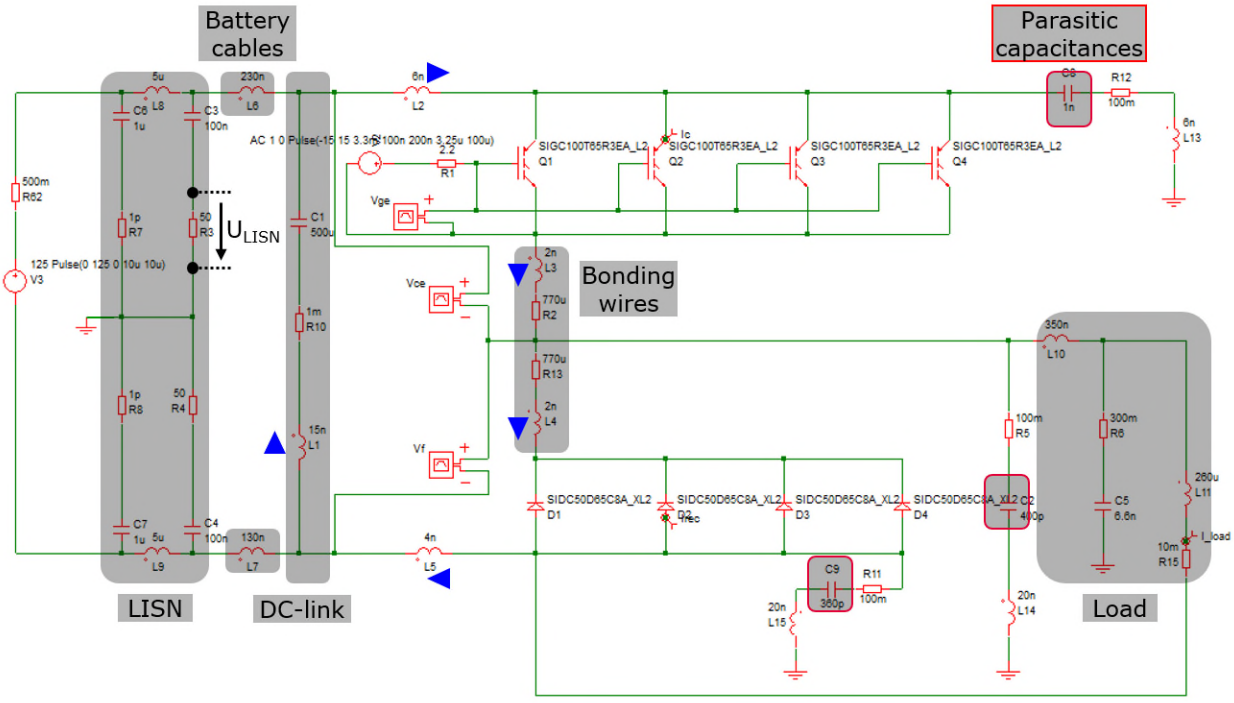


Fig. 4-9: Refined simulation model in mix-mode (CM + DM) with Infineon chip models integrated

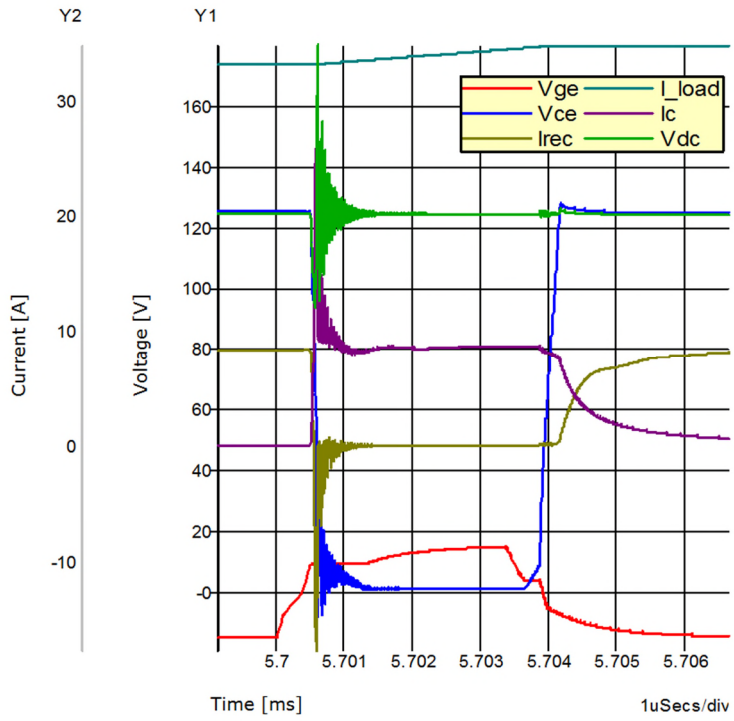


Fig. 4-10: Simulated, more realistic switching curves from the refined simulation model (Tj = 25°C)

It is noticed that the voltage fluctuation of the DC-link is also reproduced by the simulation during the turn-on and -off of the IGBTs, which means the main source of the DM interferences is also compacted into the system. The green curve in Fig. 4-10 shows how the IGBTs' switching-on and -off processes cause respectively a strong and a weak fluctuation in the DC-link capacitor. This corresponds to the measured U_{DC} curve in chapter 4.2.1 (see Fig. 4-8 left). This strong fluctuation is actually a RLC oscillation with the resonance frequency of 24 MHz. Its origin is investigated in this work and can be explained like this: When the HS IGBT is turned on and the LS diode reversely recovers, the stray inductance of the power module and the DC-link (L1, L2…L5 in Fig. 4-9, marked by blue triangles), combined with the parasitic capacitance of the IGBT and diode chips together, composite a LC oscillation loop. The stray inductance, according to the simulation model, has a sum of 29 nH. The chip capacitances, which are voltage dependent, can be referred from Table 7 in chapter 5.1.2, that makes a sum of 1.5 nF. An oscillation of 24 MHz in the DM loop, whose amplitude is damped down by the resistance as time goes on, is therefore in the simulation caused. Thus, a peak of 24 MHz in the EMI spectrum can be observed in Fig. 4-11.

The simulations of the U_{DC} fluctuations indicate that the refined simulation model simultaneously contains both interference modes (CM and DM). Also, the analysis time is shortened, because the processing and combination of the simulation results obtained beforehand by the two separated simulation models are now no longer necessary.

In order to verify the correctness and accuracy of the refined simulation model, the simulation result and measurement result in spectra are compared. In Fig. 4-11 the blue curve represents the measured spectrum in the buck-converter operation (single-phase). The simulation in red color reproduces such operation of the power module. A good correspondence between both curves can be observed. This means that the refined simulation model using the Infineon chip models with consideration of power module's relevant parasitic parameters, as well as the

relevant system components, turns out to be capable of characterizing the essential trends of the conducted EMI.

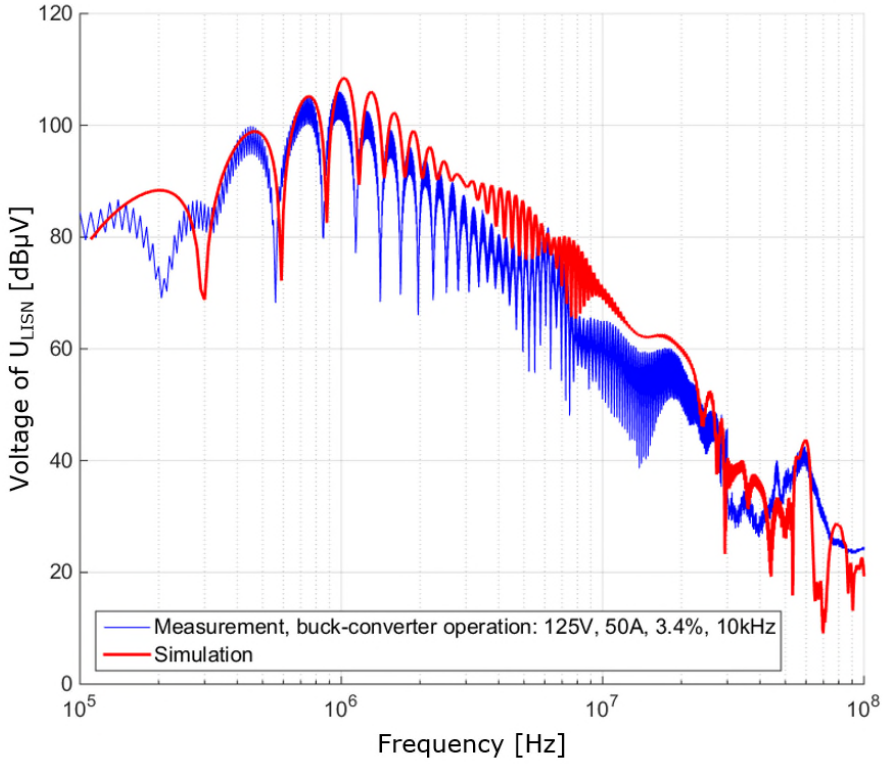


Fig. 4-11: Comparison of the measured (blue) and simulated (red) conducted EMI spectra

5. A new EMI measurement method for automotive power modules

On the power module level, the "state-of-the-art" EMC tests are currently being carried out in a simplified, generic system environment. This means that the power module is actively operated under the circumstance where both the power electronics components (DC-link, filters and inverter) and the system environment parts (LISN, E-machine, HV cables and housing) are simplified if compared to a real vehicle [37]. As it is hard in the early development phase to get enough information about the EMC features of the component and corresponding system (especially inconvenient by extracting the parameters of the equivalent circuit models [31][33][52]), it is useful to carry out additional investigations by means of using an environment-independent measurement method, which can provide information about the pure component (power module). Within the research of Kochetov and Smazinka, a novel measurement method for the power electronic is presented. It allows an environment-independent characterization of different power modules.

From the power module manufacturer's point of view, the following approach is proposed: The power module manufacturer will perform a basic EMI qualification of its products independently on the system. Based on the research of Kochetov and Smazinka, the usage of a new test procedure makes it possible to estimate the conducted EMI performance of the power module without building the whole test setup like in a conventional EMI measurement. This characterization can subsequently be used in the phase of converter development to select a suitable device and evaluate the expected effort to comply with EMC standards.

As illustrated in Fig. 5-1, the receiver in an electrical system will receive the interference current, when the emission from the interference source is transmitted by the admittance network during the signal transmission. The interference voltage can even be amplified in specified frequency areas, where the LC-resonances of the admittance network [59] exactly take place. The main idea of the novel test procedure in this chapter is to measure the frequency-dependent transfer admittance of the power module under certain circumstances, in order to find the critical resonance points that would later lead to a higher interference spectrum and the deterioration of the conducted EMI performance in the operating state.

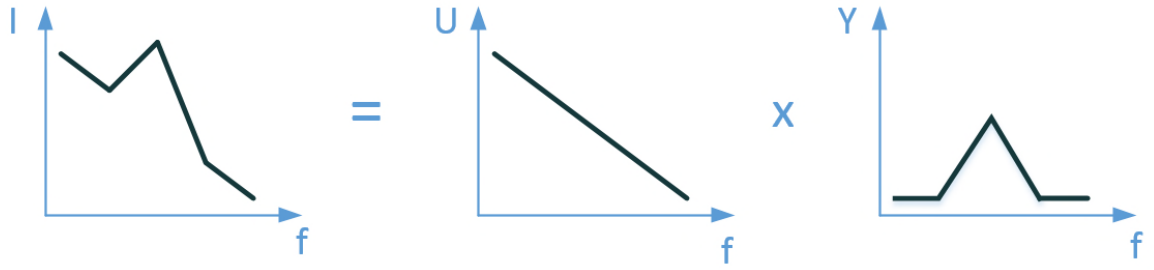


Fig. 5-1: Decomposition of the interference current (left) in frequency domain: the emission voltage (middle) is transmitted and amplified by the admittance network (right)

5.1. Parameterization and high frequency modeling of the power module

In the work of Kochetov and Smazinka in [37], the measured transfer-admittance curves of a half-bridge in Infineon® HybridPACK™2 module [84] are used as an example to describe the EMI characteristics of the power module. Fig. 5-2 shows the equivalent circuit of this transfer-admittance measurement for a half-bridge in [37], where the signal pin, terminals and heat sink of the power module are used to conduct the input and output signals. In the measurement result that is shown in Fig. 5-4 bottom, there are two obvious peaks in the curves that indicate two critical resonance points caused by the power module itself. In order to locate the origin of these resonances and continue the research, it is necessary to model a half-bridge in the power module. The relevant parasitic components are due to be parametrized in advance.

For complex modeling, it is possible to use the Maxwell Q3D extractor to model the parasitic inductance and capacitance [32]. In this work, since the most relevant elements of this model are only module pin inductances, chip capacitances and DCB parasitic capacitances, they are parameterized through the procedures described in the following sub-chapters.

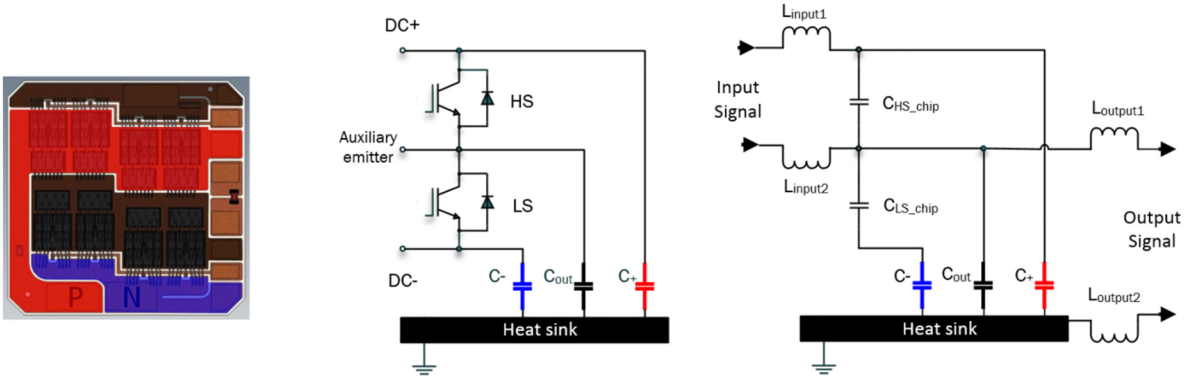


Fig. 5-2: Half bridge with IGBTs and diodes: physical assembly (left), circuit including coupling capacities to heatsink (center), equivalent circuit for EMI characterization with blocking devices (right)

5.1.1. Module Pin inductances

The measurement of the power module's transfer-admittance in [37] could not be implemented without an appropriate connection between the module and a VNA (Vector Network Analyzer). The module pins with certain inductances (specified in Fig. 5-2 as $L_{input1/2}$ and $L_{output1/2}$) enable the signals to be imported into the power module, transferred and then received again. Usually the inductances could be calculated for conductors with different shapes [34][35]. In this work, they are estimated by using the formula (5-1) shown below. This formula given by [36] is defined to calculate the pair of wires' inductances, in which the current flows through the first wire and then returns through the second one. The inductance per unit length can be calculated using the fomula, if the parameters r_0 and *a* are known. r_0 represents the radius of the wire while *a* represents the distance between two wires. Finally, the inductance can be calculated by further knowing the length of the wire. The dimensions of the pins in Fig. 5-3 as well as the calculated inductances are listed in Table 6. The horizontal distance between the load pin of the power module's middle phase and the connector of the power module's substrate (as shown in Fig. 5-3 on the right) measures 110 mm and is considered as the root cause for $L_{output2}$ in the calculation.

$$L_p = \frac{\mu_0}{\pi} \cdot \left(\frac{1}{2} + \ln\left(\frac{a}{r_0} \right) \right) \qquad \textbf{(5-1)}$$

Table 6: Needed parameters and calculated inductances

	L_{input1}	L_{input2}	$L_{output1}$	$L_{output2}$
Length [mm]	18.3	18.3	Approx. ⅓ L_{input1}	15
a [mm]	10.5	10.5		110
r_0 [mm]	2	2		1
L [nH]	**15.8**	**15.8**	**5.3**	**31.2**

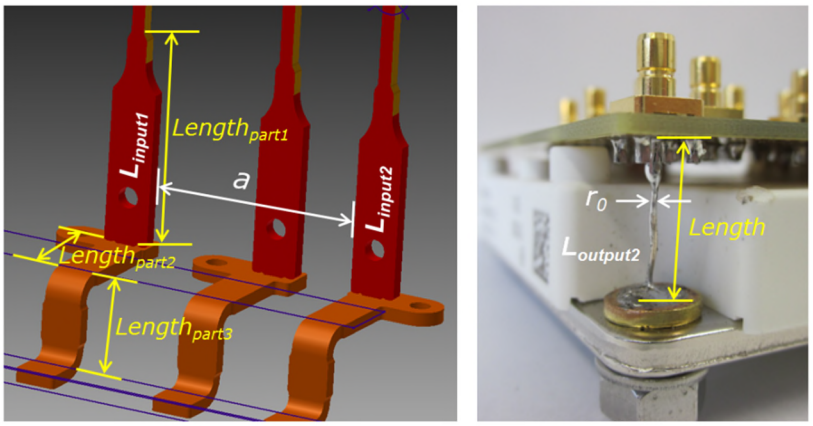


Fig. 5-3: Calculation of the inductances that are involved in the measurements in [37]

5.1.2. Chip and DCB parasitic capacitances

It is well known that the parasitic capacitances of semiconductor chips are voltage dependent. Generally, the IGBT capacitance consists of three sub-capacitances between its Collector, Gate and Emitter [16]. For the power module manufacturer these sub-capacitances can be obtained by certain measurements on chips. In Table 7 the values of these sub-capacitances are specified as C_{GC}, C_{GE} and C_{CE}. In order to obtain the total capacitance of the IGBT, the C_{GC} and C_{GE} should first be connected in series and then connected parallel to C_{CE}. The sum capacitance inside a half-bridge of the power module should be calculated by multiplying with 4, since there are 4 IGBTs and 4 diodes running paralleled in each side (High-Side and Low-Side) of the bridge.

As demonstrated in Table 7, the semiconductor chips without DC voltage stress show a much bigger capacitance. However, the capacitances reduce rapidly if DC voltage is being applied to the chips. They decrease continuously if the DC voltage is being increased whereas the dependency grows weakly if the voltage is higher. In the HV electrical drive system of vehicle, the capacitances could almost be considered as constant when the DC voltage is higher than 100 V. Generally, the power module in a vehicle operates at high-voltage under several hundreds of volts. In the paper, this specific situation is reconstructed using the conventional conducted EMI measurement (designated as “active measurement”). Unfortunately, the passive measurements in this dissertation can only be carried out by applying a DC voltage of 25 V for safety reasons. This would cause the deviation of the chip capacitances and further lead to different passive and active measurement results (as specified in chapter 5.3).

The parasitic capacitance of the DCB describes the capacitive coupling of the power module’s HV-System against the ground. It mainly depends on the thickness of the ceramic as well as the size of the copper areas. In Fig. 5-2 the DCB of a power module is divided into 3 areas by using 3 different colors. The voltage potential of each area differs from one another if the power module is being operated. The 3 capacitances specified as C_{+}, C_{-} and C_{out} [1] can be easily calculated as parallel plate capacitors since the ceramic thickness and the copper areas are well-known parameters for the power module manufacturer. The calculated results in this dissertation run as follows: C_{+} = 0.36 nF, C_{-} = 0.12 nF, C_{out} = 0.39 nF.

Table 7: Voltage-dependent parasitic capacitances of the IGBT and diode chips in Infineon® module

	IGBT				**Diode**	**HS / LS Chips sum capacitance in Module**
DC-Voltage [V]	C_{GC} [nF]	C_{GE} [nF]	C_{CE} [nF]	**C_{sum} [nF]**	**C_{Diode} [nF]**	**$4\times(C_{sum}+C_{Diode})$ [nF]**
0	5	12.7	0.4	4	1.84	23.36
12.5	0.52	12.6	0.06	0.56	0.39	**3.8**
25	0.38	12.6	0.04	0.41	0.29	2.8
125	0.20	12.5	0.03	0.23	0.14	**1.48**
200	0.18	12.4	0.02	0.2	0.11	1.24

Thus, a simulation model with the aforementioned parameters is established. The transfer admittance of this model shows a good correlation with the measurement results as shown in [37]. The two peaks in Fig. 5-4 indicating two critical resonance points are reproduced in this simulation. Two different kinds of resonant loops generated by the power module itself are thereby located.

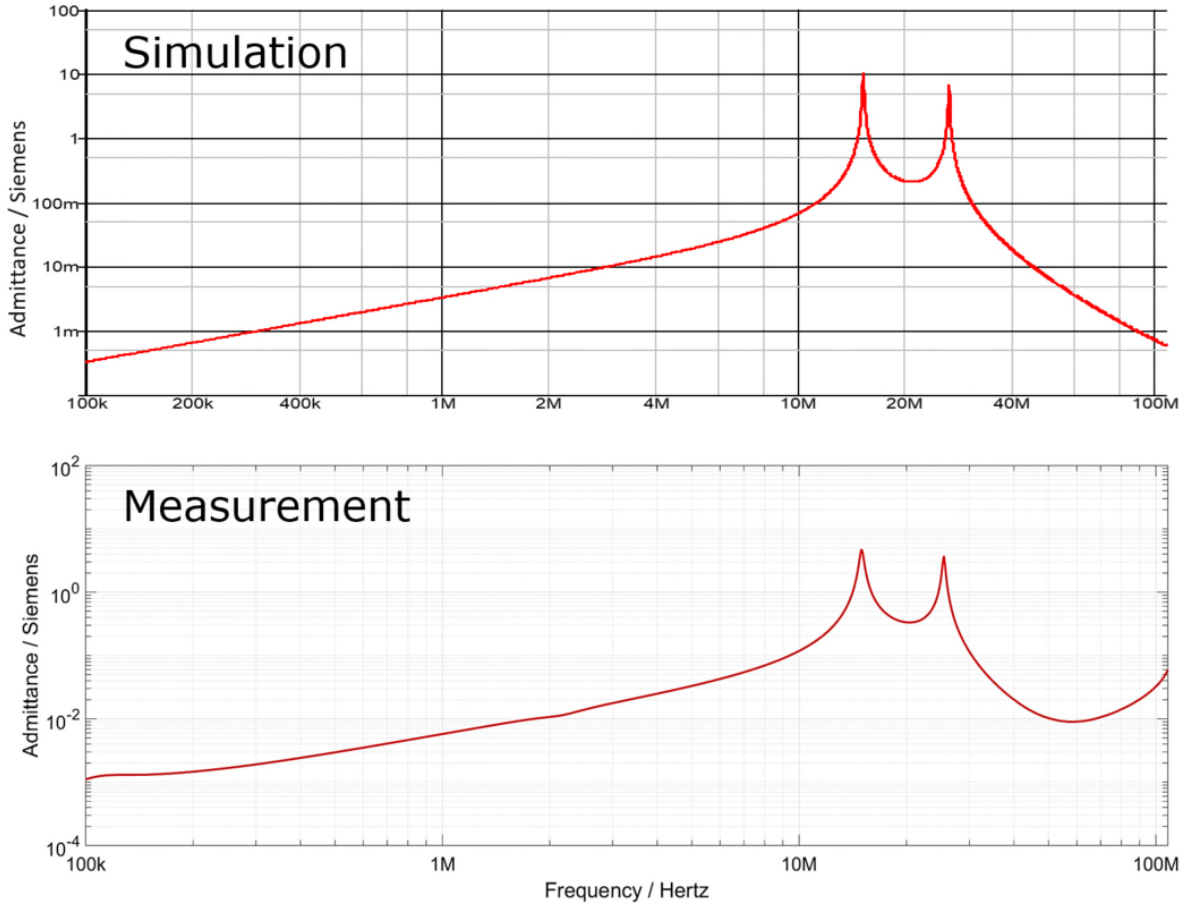


Fig. 5-4: Simulating (top) and measuring (bottom) the transfer-admittance of a half-bridge in power module, wherein the High-Side chips of the half-bridge are set under the DC voltage of 25 V

5.2. Mechanism and setup of the passive measurement

The main motivation of the passive measurement procedure is to locate and rebuild the critical resonance loops which would appear in the power module during operating state and lead to a higher interference spectrum.

The passive measurement in this paper can be considered as a two-port network investigation, its mechanism can be explained through Fig. 5-5. It is assumed that the interference source originates from the VNA, which is connected between the DC+/- of the power module. It stimulates the input signal into the module's HV terminals DC+/- through the contacting adapter

shown in Fig. 5-6. The stray inductances L'_{input1} and L'_{input2} for this connection are respectively approx. 10 nH. The calculation method of the stray inductances has been mentioned in 5.1.1. The signal transfers to the half-bridge of the module, whereby both IGBTs in the half-bridge are statically blocking a DC voltage of 25 V from the “combined BiasTee with Balun circuit” as demonstrated in [37]. The 25 V voltage is equally divided into two parts (each 12.5 V) as the semiconductors on both sides of the half-bridge are symmetric. In the half-bridge there exist parasitic capacitances of DCB against ground, they are summarized as C_{+}, C_{-}, and C_{out}. As discussed in chapter 5.1.2, these three capacitances are essential parts of the resonance loop as they are charged and discharged against ground during IGBT switching. According to the EMI mechanism, the interference spreading through the DCB capacitances will somehow return to its source in order to close the electric circuit. During the active EMI measurements, the LISN is usually inserted for the purpose of defining the return path of the interference and enabling the measurement [67]. Such a path should also be defined for the sake of the passive measurement introduced in this dissertation to complete the loop during the measurement and obtain correct resonances. As a result, an impedance called “ALISN (Artificial LISN)” is inserted, connecting the heat-sink and the electric circuit of the power module. Similar to the structure of a LISN, the ALISN consists of two capacitances C_{ALISN+} and C_{ALISN-} of 100 nF, as well as an inductance L_{ALISN} of approx. 5 nH rebuilding the ground strap from the active EMI measurement. The real LISN for automotive application consists of another inductance (5 µH) and capacitance (1 µF) in series connection. There are two reasons why the inductance inside the LISN is irrelevant to the research of this dissertation: First, the L-part of the LISN is only intended to prevent the interference from flowing into the feeding network which is not present in the passive measurement. Second, the L-part of the LISN normally has an inductance of 5 µH in automotive application. Within the affected frequency area of the CM resonance (usually ranging from 10 to 100 MHz), where the power module’s parasitic capacitances play a role, the L-part of the LISN would act as enormous resistance to block the CM current. However, the ground strap is often used in the active EMI measurement to ground the power module’s housing. The leakage inductance of the ground strap (usually with a value of some ten nano-Henrys) should be considered as the actual main L-part in the resonance loop. The output port of the network is set to be the plus and minus poles of one ALISN resistor of 1 Ω.

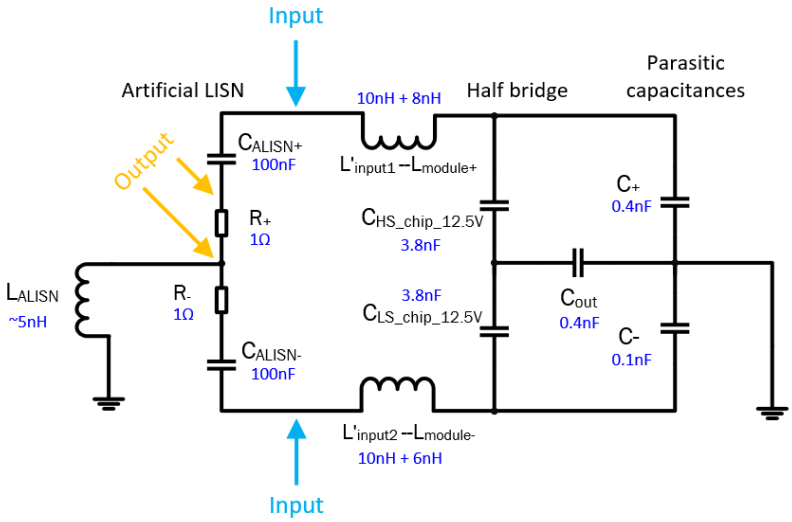


Fig. 5-5: Schematic diagram of the most relevant parameters in the passive measurement

The ALISN for the passive measurement has been implemented in the contacting adapter shown in Fig. 5-6 to provide the connection between the power module and the VNA. The ALISN has been equipped with wires providing the L and SMD capacitors on the adapter PCB, as highlighted in yellow in Fig. 5-6. The leakage inductance, determined by the length and width of the wire, replaces the role of the ground strap used in the active EMI measurement. After the CM loop is completed by ALISN the setup emulates the measurement circuit with interference receiver.

As mentioned before, due to the voltage-dependent capacitance of the collector-emitter path of the IGBT chip, a BiasTee combined with the Balun (balance to unbalance) for DC voltage feeding of 25 V has been added into the measurement setup. Thus, it is possible to "bias" the power semiconductor to take the voltage-dependent collector-emitter capacitance, as well as the associated change in the resonance frequency, into account. To ensure reliable electrical connections, some special SMT-connectors are used in the adaptor. It is well accepted that the calibration of the VNA exerts a fundamental influence on the measured results. In this research, one has to make sure that the signals are exactly propagated from the measuring instrument (the VNA) to the respective pins of the power module. The usage of the calibration standard UOSM (Unknown through-Open-Short-Match) [81], in combination with the “Fixture compensation” directly integrated in the measurement adapter, as highlighted in white areas “Open”, “Short” and “Match” in Fig. 5-6, makes it possible to fulfil the requirements. Each port from the VNA must be calibrated using this structure before the passive measurement is carried out. As a result, the compensation of the signal propagation times can be made precisely up to the connection pin of the power module. This provides a sufficient accuracy up to approx. 110 MHz.

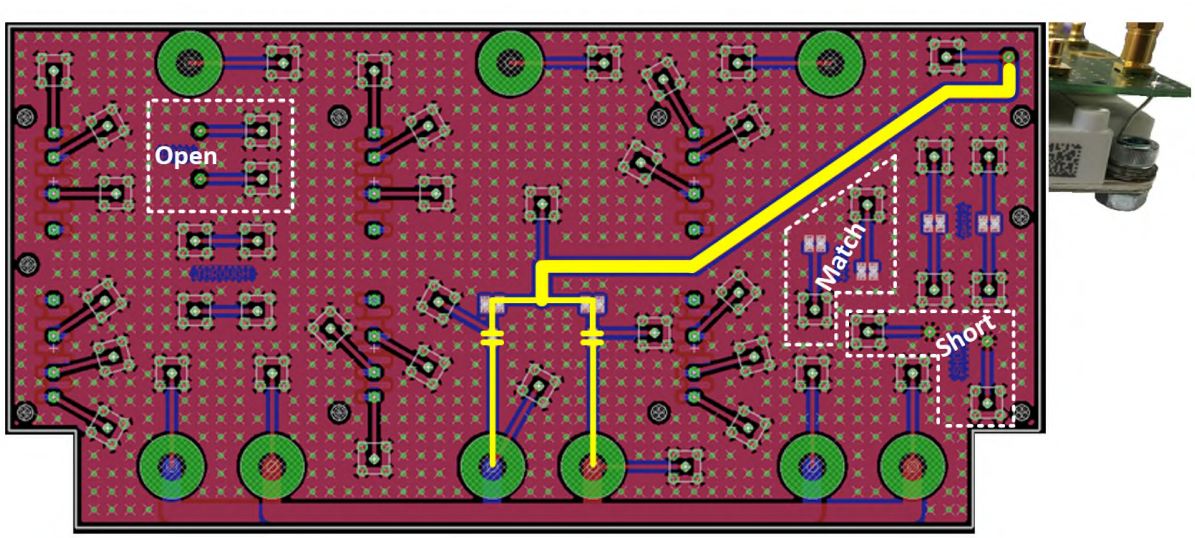


Fig. 5-6: Realization of the defined artificial LISN (ALISN) on the measurement adapter through the connection marked in yellow and the "fixture compensation" in white

After introducing the setup, the critical resonant loops in the passive measurement and their correlation to those in the active measurement are further investigated.

The network in active measurement is normally divided into differential-mode (DM) and common-mode (CM) for analysis. The mechanism of the two interference modes can be referred from chapter 2.1.2. By DM mode, the interference current flows within the HV system to build up a closed loop. In this work, that means the EMI current transfers between DC+ and DC- of the system, involving the DC-link, the stray inductances of power module, the chip capacitance and partially the power module parasitic capacitances (see Fig. 5-7 a)). Since the module is in operating state, the switched-on HS IGBT of the half-bridge can be considered as conducting without chip capacitance. Meanwhile, the LS IGBT and its parallel connected diode in blocking state can be considered together as a capacitor whose capacitance depends on the voltage of the DC-link (125 V for active measurement, see Table 7). The capacitance of the DC-link itself can be eventually neglected, since it is generally set at milli-Farad range and thus by several orders of magnitude higher than the other chip and parasitic capacitances involved in the network, at times when the inductive part of its impedance is considered in $ESL_{DC\text{-}link}$. By CM mode, as illustrated by Fig. 5-7 b), the EMI current transfers though both DC+ and DC- in the same direction, then returns to close the loop by flowing across the GND. The main parts involved in CM mode are accordingly: the LISN capacitances, the stray inductances and parasitic capacitances of power module, as well as the stray inductance of the ground strap. The DC-link and chip capacitance turn out to be irrelevant in the CM loop.

The network in the passive measurement, which is shown in Fig. 5-5, is divided in differential-mode (DM) and similar-common-mode (SCM) for analysis. The similar-common-mode (see Fig. 5-9) is so designated because of following reasons: On one hand, the resonant loop of this mode is similar to the aforementioned CM loop, involving the components, which are normally relevant only in common-mode but not in differential-mode, such as the inductance for rebuilding the ground strap from the active measurement (L_{ALISN}). On the other hand, the relevant emission current flowing in this mode is not exactly the typical common-mode current, since the SCM emission currents of DC+ and DC- sides in the HV system do not flow towards one same direction. The real CM loop of active measurement is not possible to be rebuilt

through passive measurement, because in the former case, the CM interference source is usually defined by potential fluctuation against ground due to the charge and discharge of the power module's parasitic capacitances (mainly C_{out}); while in the latter case, the input-port of VNA is set between DC+ and DC- to play the role of interference source.

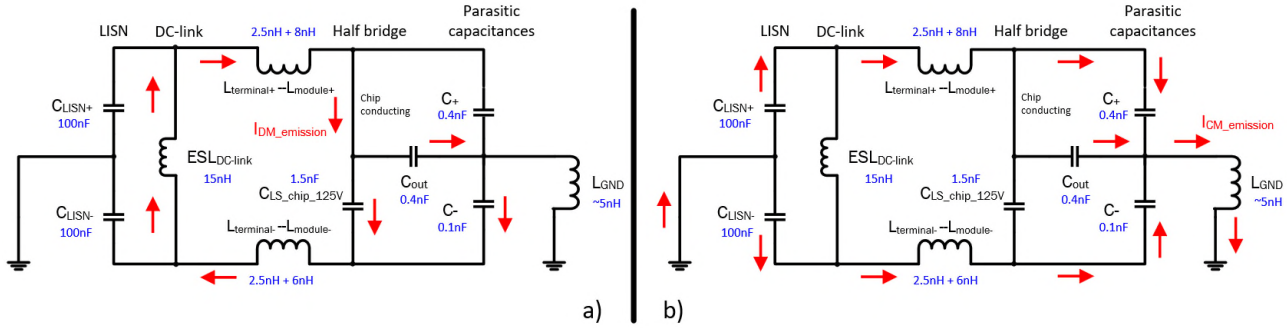


Fig. 5-7: DM a) and CM b) EMI current loops in active measurement structures (red arrows indicate the interference current paths)

For DM analysis, the relevant DM resonant loop of active measurement in Fig. 5-7 a) has been abstracted and compared with that of passive measurement in Fig. 5-8. The $ESL_{DC\text{-}link}$ normally with a value of some ten nano-Henrys can be located out in the datasheet of the capacitor manufacturer (in this work 15 nH for the EPCOS® film capacitor *B25655J4507K* [71]). Additionally, the stray inductance resulting from the connection between the DC-link capacitor and the power module usually amounts to 2 to 4 nH (in this work 2.5 nH), which would play a minor role in the analysis. As mentioned before, the interference source of the passive measurement actually originated from the VNA. It is connected between the DC+/- of the power module through the aforementioned adaptor. For this structure there is no DC-link being present. As shown in Fig. 5-8 b), both IGBTs in the half-bridge are statically blocking a DC voltage of 25 V. As can be seen in Table 7, the capacitance of the chips from each half-bridge side under 12.5 V (3.8 nF) is about twice the capacitance of those under 125 V (1.48 nF). However, the series-connection of the HS and LS chips under 25 V cuts the sum of the capacitance in half to 1.9 nF. After taking along the parallel-connected parasitic capacitances (C_{-}, C_{+}) into consideration, it proves that the equivalent capacitances of the DM loop for both passive and active measurements are not greatly different from each other. A complete DM loop is formed in the passive measurement circuit when the two series connected capacitors of 100 nF from the ALISN are involved. Finally, since the sum of the stray inductances in passive measurement (34 nH due to L'_{input1}, L'_{input2}, $L_{module+}$ and $L_{module-}$ in series connection) happens to be equal to the sum of $ESL_{DC\text{-}link}$ (15 nH) and the module (plus terminal) stray inductances (19 nH) in series connection, the DM loop in passive measurement with resonance frequency of 19.3 MHz could almost virtually rebuild the other DM loop with resonance frequency of 21.5 MHz, which appears in the active measurement.

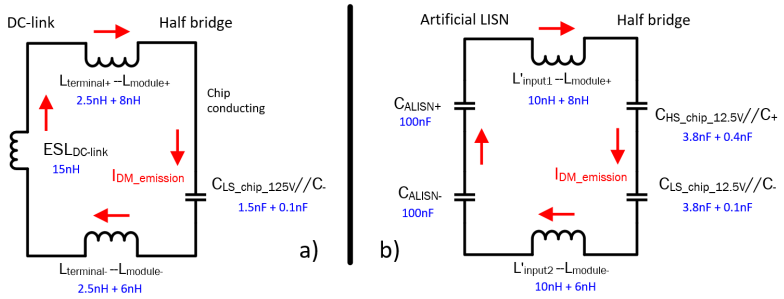


Fig. 5-8: DM resonant loops in a) active- and b) passive- measurement structures (red arrows indicate the current paths at relevant resonance frequency)

On the other hand, in consideration of the SCM resonance loop, the parasitic capacitance of the DCBs in the power module should mainly be taken into account. The comparison of the SCM loop between passive and active measurements is presented in Fig. 5-9. In both structures, the similar-common-mode emission current flows through the half-bridge and the module parasitic capacitances, then back to the LISN (or ALISN) to form the loop. Since the locations of the emission sources in active and passive measurements differ from each other, the relevant components involved to form each SCM loop are not the same. From the inductance point of view, L_{GND}, $L_{terminal+}$ and $L_{module+}$ are connected in series in active measurement, consisting an inductance of 15 nH, while in the depicted dominating loop of the passive measurement the series-connected L'_{input2}, $L_{module-}$ and L_{ALISN} form an inductance of 21 nH. From the capacitance point of view, the structure of the capacitive network in passive measurement is more complex than that in active measurement: In active measurement, the parasitic capacitance C_{out} of the DCB is parallel connected to the sum of $C_{LS\_chip\_125V}$ and C_{-} (in series), then resulting in a capacitance of 0.49 nF after connecting with C_{LISN+} in series. This structure is expressed simply as [C_{out} // ($C_{LS\_chip\_125V}$ -- C_{-})] -- C_{LISN+} = 0.49 nF, in which the "--" symbol represents series connection and the "//" symbol means parallel connection. In passive measurement however, the capacitive network turns out to be C_{-} // {$C_{LS\_chip\_12.5V}$ -- [C_{out} // ($C_{HS\_chip\_12.5V}$ -- C_{+})]} -- C_{LISN+} = 0.72 nF. As a result, the SCM loop of active measurement can come up with a resonance frequency of approx. 58 MHz, while by passive structure the value is about 41 MHz. This deviation can be confirmed in the next section (see Fig. 5-11 a)).

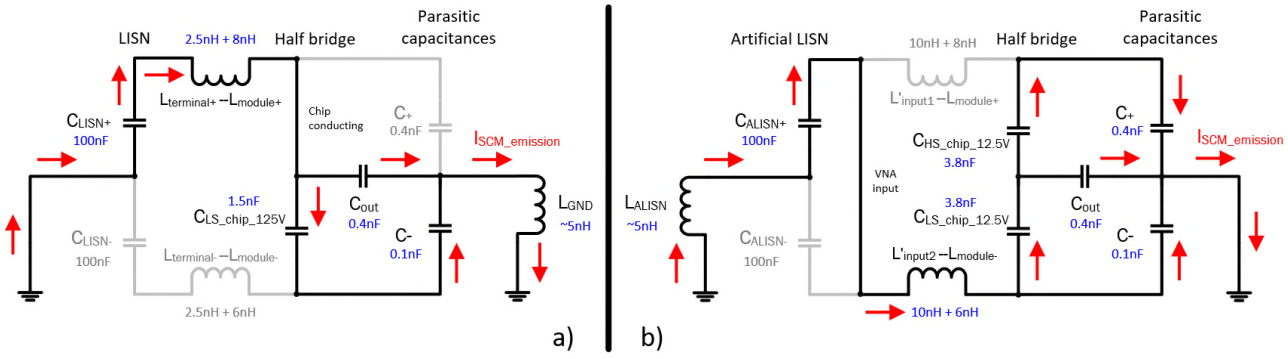


Fig. 5-9: SCM resonant loops in a) active- and b) passive- measurement structures (red arrows indicate the current paths at relevant resonance frequency)

5.3. Verification of the passive measurement results

After the different resonance loops being rebuilt as analyzed, the verification can be carried out in this section. The proposed concept is validated by comparing the results of passive and active measurements. Since the active measurement delivers the voltage drop across the LISN and the passive measurement admittances, the latter has been transformed as shown in Fig. 5-10: The admittance curve *Y* from the passive measurement is multiplied by the spectrum *U* of a defined trapezoidal interference source with certain rise- and fall-times (in this work t_{rise} = 100 ns and t_{fall} = 200 ns according to the IGBT double-pulse test). The product *I* is then compared with the active measurement result.

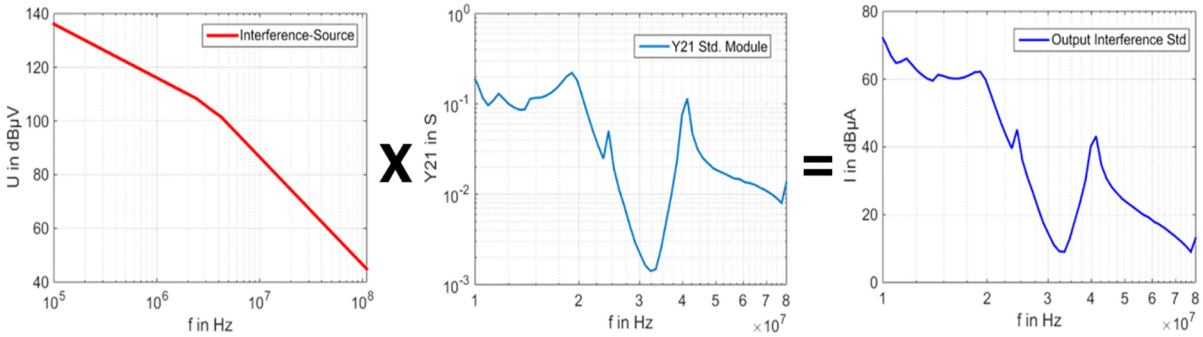


Fig. 5-10: Mechanism and method of signal processing for the passive measurement

In this dissertation, a normal HP2 module (abbreviated as Std. module) for automotive application, as well as two other EMI-optimized versions of that module, are being tested. The EMI-optimized versions are based on the standard module; additionally the Y-capacitors of 10 nF as well as 250 nF per phase are integrated between the power module's DC+/- and the heat-sink to optimize the EMI performance (details are given in chapter 6.3). Fig. 5-11 shows the comparison of the actively and passively measured curves of each DUT.

As shown in Fig. 5-11 a), the examined frequency area is firstly set between a range of 10 MHz and 100 MHz since the resonance points of the power module are approximately located within this area. The DM resonance point which appears in the active measurement at about 20 MHz is successfully rebuilt by the passive measurement. The reason for this has already been explained in chapter 5.2 (see Fig. 5-8): The DM loops in the passive- and active-measurements are almost equal to each other since the equivalent capacitances of the DM loop in both passive and active measurements are not much different from each other, and additionally the sum of L'_{input1} and L'_{input2} is also equal to the sum of $ESL_{DC\text{-}link}$, $L_{terminal+}$ and $L_{terminal-}$. As expected, a deviation of SCM resonances ranging from 41 MHz to 58 MHz can be observed at the standard module. The reason has also be explained in the previous section (see Fig. 5-9): Since the involved elements for the SCM loops in active and passive measurement structures are not the same, the resonance frequencies of the two SCM loops are destined to differ from each other.

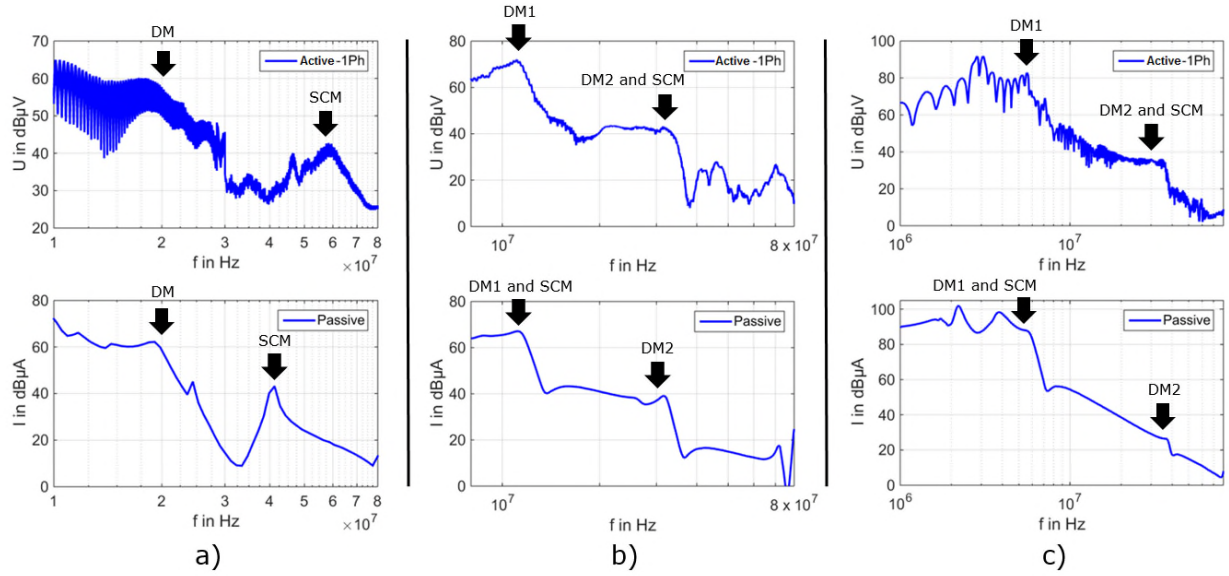


Fig. 5-11: Verification of the passive measurements: a) on a standard power module, b) on the same module with integrated Y-capacitors of 10nF and c) of 250nF

In Fig. 5-11 b), the in power module integrated Y-capacitors (10 nF per DC side) and their ESLs offer a new path running parallel to the DC-link and the module half-bridge, cutting the existing DM loop (shown in Fig. 5-8) into two newly formed loops. The schematic diagrams of these new loops (called DM1 and DM2) are presented in Fig. 5-12 a) and b) for active and passive measurement structures respectively. For DM1 in active measurement, the LC network consists of the Y-capacitances, their ESLs and other components, which means $L_{terminal+}$ -- $L_{terminal-}$ -- $ESL_{DC-link}$ -- ESL_{Y+} -- ESL_{Y-} -- C_{Y+} -- C_{Y-} forming a new loop with the resonance frequency of approx. 11 MHz. The ESL_Y of the 10 nF foil capacitor is approx. 5 to 10 nH because of the pins of foil capacitors (details see chapter 6.3). In passive measurement, the resonance frequency for DM1 is also approx. 11 MHz duo to the LC network which consists of L'_{input1} -- L'_{input2} -- ESL_{Y+} -- ESL_{Y-} -- C_{Y+} -- C_{Y-} -- C_{ALISN+} -- C_{ALISN-}. For DM2 in both active and passive measurements, the module stray inductances $L_{module+}$ and $L_{module-}$ as well as the chip and module parasitic capacitances are involved to form a loop together with the integrated Y-capacitors. The resonance frequencies of DM2 for active and passive measurements (in Fig. 5-12 a) and b)) are both nearly 30 MHz, because the only deviant parameter is the sum of the voltage-dependent chip capacitance and the parasitic capacitances, being in active structure 1.6 nF and in passive structure 2 nF. In another aspect, the deviation of SCM loops between active and passive measurements remains visible after implanting the Y-capacitors into the power module. The SCM resonant loops in Fig. 5-9 for active- and passive- measurements can be so modified, as if the module DCB capacitances C_+ and C_- are respectively parallel connected to a capacitance of 10 nF (and its ESL). The capacitive network of active measurement then turns out to be $[C_{out}$ // $(C_{LS\_chip\_125V}$ -- $C_{Y-})]$ -- C_{LISN+} = 1.6 nF, while of passive measurement it can be simplified as C_{Y-} -- C_{ALISN+} = 9.1 nF (the other capacitive parts parallel to C_{Y-} are much smaller thus neglected). As for the inductive network, the Y-capacitor brings extra ESL element, which consists $L_{terminal+}$ -- $L_{module+}$ -- ESL_{Y-} -- L_{GND} = 20 nH in active measurement and L'_{input2} -- $L_{module-}$ -- ESL_{Y-} -- L_{ALISN} = 26 nH in passive measurement. Therefore, after integrating the Y-capacitors of 10 nF (per DC side), the SCM resonance frequencies of both active and passive measurements turn out to shift towards lower frequency band: In active measurement it shifts from 58 MHz to approx. 28 MHz, next to the DM2 resonance point of 30

MHz, while in passive measurement the shifting goes from 41 MHz to approx. 10 MHz, close to the DM1 resonance point of 11 MHz. The tendency is consistent in both active and passive measurements, that the integration of Y-capacitors of 10 nF (per DC side) can cause a shifting effect of the SCM resonance frequency by approx. 30 MHz towards lower frequency area.

The examined frequency area of the EMI-optimized module is then extended to a range between 1 MHz and 100 MHz due to the integration of larger Y-capacitors of 250 nF per DC side, because of the resonance shifting effect which is confirmed by last paragraph. The effective capacitance of each CeraLink™ capacitor is only 70 nF due to the DC voltage bias of 125 V (see chapter 6.3). In Fig. 5-11 c), the general trends of both measurement curves show a reasonable correlation. The DM1, DM2 and SCM resonance points are still visible. Similar to analyzing the previous power module with integrated foil capacitors of 10 nF (per DC side), by using the schematic diagrams in Fig. 5-12 with the parameters marked in red for the CeraLink™ capacitors of 250 nF, it can be calculated that the resonance frequency by DM1 for both active and passive measurement structures is around 5 MHz, while by DM2 it amounts to approx. 30 MHz. The shifting effect of the SCM resonance frequencies of both active and passive measurements can also be observed. In Fig. 5-11 c), the peak around 30 MHz for active measurement and the peak around 5 MHz for passive measurement, whose shapes are not as sharp as a normal resonance peak, indicate the overlapping of the SCM peak on corresponding DM peak.

In conclusion, it is justifiable to say that the DM resonance points in active measurement can be successfully rebuilt by passive measurement; jet the deviation of the SCM resonance points is unavoidable. This results mainly from the composition difference of each SCM loop in active and passive measurements because the positions of the emission sources for the two measurement structures are not identical. However, it can be confirmed from both active and passive measurement, that extra capacitive connections in the power module between the HV-system and the heat-sink would lead to shifting the resonance points into lower frequency areas. Although further studies on these issues is in need, the passive measurement results have proven to be able to show a good qualitative and partially quantitative correlation with the active measurement results.

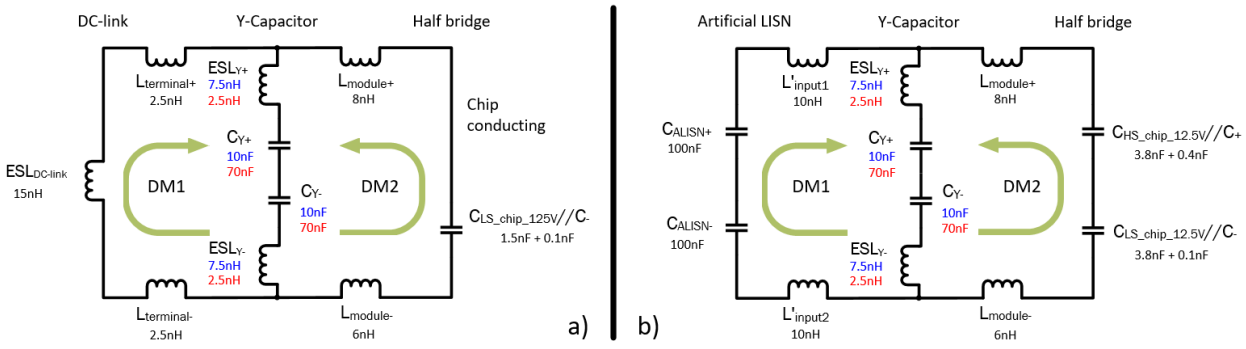


Fig. 5-12: Schematic diagrams of the newly formed DM1 and DM2 loops after Y-capacitor insertion in a) active- and b) passive- measurement structures

6. EMI optimization in automotive application with special consideration of power module

In this dissertation, in order to improve the EMI performance of electrical drive system in vehicle, the research focuses on the main interference source itself: the power module. Infineon®'s HybridPACK™ 2 (abb. as HP2) is selected as the test subject, to develop EMC-compliant design concepts for power modules and packages.

The HP2 [84] is an automotive qualified power module designed for hybrid- and electric vehicle applications in a power range up to 100 kW continuous power. The module accommodates a 3-phase configuration of Trench-Field-Stop IGBTs and matching Emitter Controlled diodes, which are designed for 150°C junction operation temperature. Maximum chip ratings are 800A of nominal current and 650V of blocking voltage. The pin-fin baseplate makes it suitable for direct liquid cooling in the drive train system. The driver stage PCB can be connected on the top of the module.

The HP2 module is designed for automotive applications with the focus of high power density, thermal cycleing capability and efficiency. From an EMC perspective, lower switching losses correlate with a higher switching speed, or larger $\mathrm{d}v/\mathrm{d}t$, $\mathrm{d}i/\mathrm{d}t$ with higher EMI. It is therefore worth investigating the development of an EMI-optimized version of the HP2 without reducing its power density and efficiency. In this dissertation, the developed and realized EMI optimization concepts for the inherently low-interference power modules can be summarized as follows:

- Concept 1: Symmetrization and reduction of coupling capacitances / leakage inductances through optimized DCB layout
- Concept 2: Placing extremely low-impedance X-capacitors directly in the power module
- Concept 3: Placing bare-die-shaped snubbers directly in the power module
- Concept 4: Placing extremely low-impedance tied Y-capacitors directly in the power module
- Concept 4*: Placing extremely low-impedance tied Y-capacitors with voltage class of 2 kV directly in the power module

The optimization process is illustrated in Fig. 6-1. From left to right the actions were carried out step by step. Initially, the DCB layout of the module was changed, under the condition that the pin positions of the power module to the outside connections (respectively DC +/-, C, G, E of HS and LS etc.) remain unchanged. The new layout "Opt_Zero" was developed, in that the parasitic capacitances / leakage inductances of the DC+ and DC- sides were symmetrized (C_{+} = C_{-}, L_{+} = L_{-}) and the C_{out} (see Fig. 5-2) was reduced as much as possible. Next, the capacitors from Epcos® were placed directly on the specially scheduled free space of the new DCB (marked in red circle in Fig. 6-1). The series "Opt_X_" has been created with various values of

the soldered capacitors (e.g., 1 µF, 0.5 µF and 0.25 µF), whereby the combination of the concept 1 and 2 is realized. The Epcos® capacitors act as X-filters because they can attenuate the DM interference of the system. Last, two bare-die-shaped snubbers from Fraunhofer IISB were used in parallel to the HS and LS chips so that the chips switch in a softer way. By combining the concepts 1, 2 and 3, the series "Opt_XS_" was created, where "XS" indicates the combined solution of the X-filter and the snubber-filter.

In the course of the research, it turns out that next to the use of the X-capacitors, the use of Y-capacitors can lead to even better results. A combination of the concepts 1, 2 and 4 was therefore successfully realized under consideration of the module compaction (Fig. 6-1 right above). Because of the additional electrical connection caused by the Y-capacitors between the HV system and the substrate of the power module, the insulation class of the module is now limited by the insulation class of the Y-capacitor. According to Epcos®, the CeraLink™ DC-link or snubber capacitors are still in development stage during this work. The conditions for Y2 (5 kV for indirect lightning strike) are not fulfilled. In the HV vehicle electrical system measurements in laboratory, only combined with appropriate protection and monitoring measures, the specified voltage strength of 900 V can be used for test purposes. Considering the requirements of the EMC test for vehicles, these modules, which fail to fulfill the insulation class of at least 2 kV, could not be tested on the system level. Instead the foil or ceramic capacitors with the Y2 voltage class were used as the Y-capacitors in the power module (Fig. 6-1 right bottom).

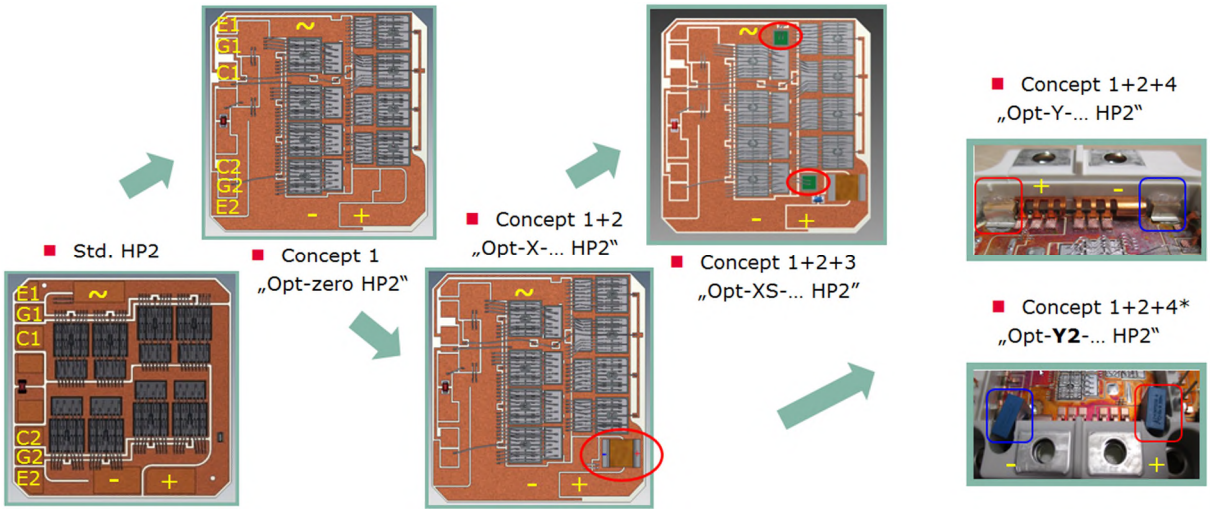


Fig. 6-1: Development and realization of various technology demonstrators with integrated measures for inherently low-interference power modules

The solutions were extensively tested and evaluated. The module variants and the characterization scope are summarized in Table 8; The details of the electrical characterization as well as the comparison of the module variants are explicated in chapter 6.1 to 6.3; the evaluation of the concepts for inherently low-interference power modules by different sorts of criteria is presented in chapter 6.4.

Table 8: Status summary of the EMI-optimized HP2 variants

Module Variants	Optimized by	Switching behavior measurements (Double-pulse) [125V] [25A, 50A, 100A, 200A]	1-phase active conducted EMI measurement	3-phases active conducted EMI measurement
Opt_Zero	Concept 1	☑	☑ [125V, 50A]	☑
Opt_X_1µ	Concept 1+2	☑	☑ [125V, 50A]	☒
Opt_S_5n5	Concept 1+3	☑	☑ [250V, 50A]	☑
Opt_XS_20n5n5	Concept 1+2+3	☑	☑ [250V, 50A]	☒
Opt_XS_500n5n5	Concept 1+2+3	☑	☑ [250V, 50A]	☒
Std_Y_1µ	Concept 4	☒	☑ [250V, 50A]	☑ (Not suitable for vehicle tests because of insufficient insulation class)
Opt_Y_250n	Concept 1+4	☑	☑ [250V, 50A and 125V, 50A]	☑
Opt_Y2F_10n	Concept 1+4*	☑	☑ [250V, 50A and 125V, 50A]	☑
Opt_Y2K_10n	Concept 1+4*	☑	☑ [250V, 50A and 125V, 50A]	☑

☑: Done / Yes
☒: Measurements not performed
Remark: Variant named after Opt_xx(Zero/X/XS/Y/Y2)_xx(Capacitance value)

6.1. EMI-Optimization of the module DCB layout

During the operation of the power module, the various IGBTs and diodes on the DCB are switching, which results in the changing of voltage over time. High du/dts during the switching processes lead to the charging and discharging of different copper surfaces, which are marked with different colors in Fig. 5-2 (see chapter 5.1.2).

For industrial application, Domurat-Linde has shown in [1] that by reducing the output capacitance C_{out} and increasing the symmetry of the module layout, the interfering emissions can be suppressed. Wang and Lee also propose similar theory in [56]. C_{out} is the coupling capacitance between the HS emitter and the bottom plate. If $L_+ = L_-$, $C_+ = C_-$, and $C_{out} = 0$, there will be no conversion of differential-mode to common-mode emissions happening. In this case, the inserted X-capacitor will work particularly effectively since there is no longer common-mode interference existing [57]. Fig. 6-2 left shows the optimized power module for industrial application with symmetrical DC +/- sides as well as the reduced C_{out} by flip-chip technology (from 80 pF to 5 pF). Besides the flip-chip approach, another possibility to minimize the output capacitance is given as an outlook in [1]: an additional ceramic layer can be added into the DCB, directly under the copper layer where the LS semiconductors of the half-bridge are

soldered. This proposal is successfully realized by Domes through a demonstrator in [38]. The demonstrator with the three-layer-DCB concept was developed, based on the new design criteria for IGBT modules with the benefit of fast switching without significant dynamic-overvoltage and reduced EMI. As a result, in a certain frequency area, the EMI emissions are reduced partially more than 10 dBµV for the three-layer-DCB module compared to the standard module. The proposal of Domurat-Linde, which promises less EMC noise, is therefore confirmed. However, compared to the conventional DCB structure, the additional layer will give rise to worse thermal behavior of the power module. The relevant evaluation regarding this topic is further discussed in chapter 6.4.

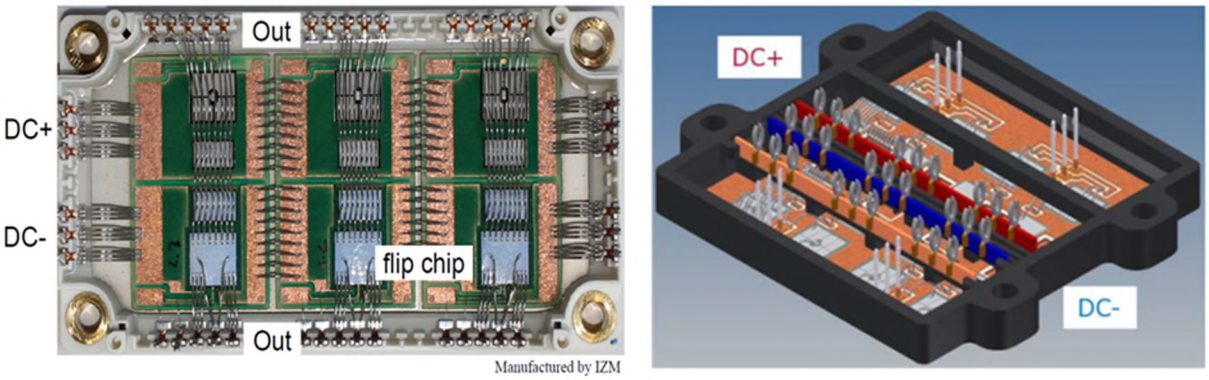


Fig. 6-2: Optimized power module by flip-chip and symmetry (left) [1] and by three-layer-DCB (right) [38]

6.1.1. Concept, explanation and realization on an automotive power module

The researched objects of Domurat-Linde and Domes were the power modules for industrial application. In this dissertation, the EMI optimization concepts are extended to cover the power module for automotive application. Based on the existing research results as well as the simulation in chapter 4, ideas and solutions are further developed.

As mentioned before, one of the prerequisites by redesigning the DCB layout of the HP2 module is that the pin positions of the power module to the outside connections (respectively DC +/-, C, G, E of HS and LS etc.) shall not be changed. Therefore, there are some specifications in the newly designed layout, which shall be explained in detail.

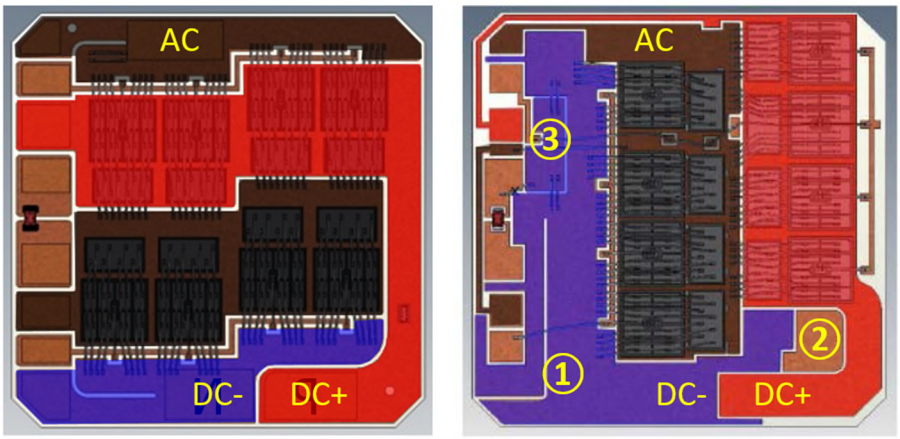


Fig. 6-3: Newly designed DCB layout for HP2 (right) concerning better EMI performance, compared to the standard layout of HP2 (left)

In the newly designed DCB layout in Fig. 6-3 right, the target of symmetrization as well as partial reduction of the parasitic capacity have been successfully fulfilled. The parasitic capacitances / leakage inductances of the DC+ and DC- sides has been designed almost equal to each other ($C_+ = C_-$, $L_+ = L_-$) of the red and blue areas. The detailed dimensions as well as parameters to calculate the parasitic capacities C_+, C_- and C_{out} are listed in Table 9. The three different copper areas can be considered as parallel plate capacitors with upper and down sides of copper layers isolated by a ceramic slice. The calculation can be done with the knowledge of the areas, the thickness of the ceramic and its permittivity ε_r.

The consideration that the external snubber or capacitor may later be integrated into the power module makes it of vital importance to reserve the place for them in advance. Hence an “island” area marked as ② in Fig. 6-3 has been designed. On this area, a snubber can be placed to connect the DC+ area (in red) and the DC- area (in blue) of the power module. The left side of the island ② is designed to be connected to the DC- copper through a few bond wires (see Fig. 6-1 bottom) or through a resistance which can additionally dampen the oscillation. Since it is not definite that this area will be used for the integration of the snubber, there has to be another equal area ③ which is pre-reserved to function as an optional “replacement area”: if external snubber or capacitor is integrated, then ② will be connected to DC-. This will lead to the growth of the DC- area and the breaking of the symmetrization of the C_+ and C_-. To maintain the balance and restore the symmetrization of DC+ and DC-, the optional area ③ shall be electrically separated from DC- by removing the bond wires which at first connect the blue area and the island ③. In this way, the sum of the blue area will remain unchanged, whether the snubber is integrated or not.

Besides, the copper area in black representing C_{out} (see Fig. 5-2) was reduced maximally. The accessory black area in Fig. 6-3 left side for the AC connection in the standard HP2 layout has been eliminated. Unfortunately, the area in black cannot be much further reduced, since the LS IGBTs and diodes must be placed on it. Because according to the design rules, the distance between adjacent chips should be at least 1 mm, when they are not separated by etching trenches, further reduction of the copper area may lead to an unreliable soldering process as well as electrical failure of the semiconductor chips.

From other points of view, for example the drive of power module, the symmetrization of the copper areas also brings disadvantages to the IGBT control. First, since the chips are

distributed in another way to the standard layout on the DCB, whereas the pin positions of the power module must remain the same, an extremely long bond wire for gate connection of the HS IGBTs is forced to be drawn from left to right side of the DCB. Besides reducing the mechanical stability, this can lead to electrical delay of gate signal to drive the HS IGBTs because of extra added inductance and resistance to the bond wire. Second, by the LS chips, since there are 4 IGBTs parallelly distributed while the auxiliary emitter of the power module is close to only one of them but far away from the others, there will be non-simultaneous driving of the 4 IGBTs due to the different inductances as well as resistances in their own gate-emitter loops of each IGBT. To reduce this negative effect, a specially designed etching trench marked as ① in Fig. 6-3 is added into the copper layout to guarantee that the IGBTs of the LS can be driven more simultaneously. The changed current-distribution on the IGBTs will be presented and discussed in the next sub-chapter.

Table 9: Dimensions and corresponding parasitic capacities of standard- and "Opt_Zero"-layout in HP2 modules (colours according to Fig. 6-3)

	Copper area [mm²]	ε_r	Ceramic thickness [mm]	C_+ [pF]	C_- [pF]	C_{out} [pF]
Standard	1315.3	9.8	0.32	356.5	119.5	387.9
	441.1					
	1431.1					
Opt_Zero	1054.9			285.9	277.4	280.6
	1023.6					
	1035.4					

To realize the newly designed layout in the power module package, the design rules from the DCB manufacturer Rogers® and from power module manufacturer Infineon® should be taken into particular consideration. According to the design rules of bonding, the loop length of the aluminum bond wire with a diameter of 400 µm should be more than 3 mm and less than 15 mm. For the "Opt_Zero" layout in this work, the maximum bond wire length is approx. 20 mm, which is slightly above the limit. This will certainly lead to the reduction of the mechanical robustness, yet it is still stable for electrical testing and investigation. Because this work focuses on the EMI performance, the power module's reliability performance is not specially considered, such as the performance in thermal shock, mechanical shock and vibration tests. If the signal pin positions on the module frame can be adjusted accordingly, the design rules of bonding can still be fulfilled to ensure the module's reliability and robustness. To ensure the reliable bonding of the power module, the positions of the bonding feet should also be taken into account. From bonding foot to chip, the distance should be kept more than 3 mm; from bonding foot to substrate edge, the distance should be no less than 0.6 mm. Furthermore, the distance of the adjacent bonding feet on substrate or on chips (IGBTs and diodes) should be kept more than 0.8 mm. According to [86], for the layout conductor (copper) with a thickness of 0.3 mm, the dimensions of the horizontal conductor width, the spacing between the conductors, as well as the etching trench width should be no less than 0.5 mm. These rules are all complied in this work.

6.1.2. Characterization of the realized automotive power module

After the construction of the special version of HP2 module, it is of utmost necessity to take a look at its electrical performance especially its switching behavior, to find out if there are abnormalities compared to the standard HP2 module. Then, as mentioned in the last sub-chapter, if the current distributions of the power module are changed, each chip can bear different currents during the operation. It is, therefore, also necessary to check if this unbalanced distribution can negatively influence the power module's switching behavior. Two kinds of dynamic measurements turn-on / -off measurement and short circuit test, are carried out to fulfill the purpose of the characterization using the measurement setup presented in chapter 2.2.2.

The turn-off / -on measurements are carried out at the same operation point as in EMI test in this dissertation (V_{DC} = 125 V, I_{Load} = 50 A, 25°C). In Fig. 6-4 the EMI-optimized version of HP2 module, named as "Opt_Zero", is compared to a standard HP2 module regarding the switching behavior. The measurement results in Fig. 6-4 verify the time delay during the turn-off of the IGBTs for the "Opt_Zero" module since the aforementioned reason, that the bond wire from the pin to the HS IGBT gate (or to the LS auxiliary emitter) in this variant is much longer than that in the reference module due to the new layout design. By remarkable time delay, the dead time setting of the inverter system has to be readjusted to avoid the HS and LS short circuit. However, the time delay by turn-off is less than 0.1 µs, by turn-on even invisible. It can be generally concluded, that the modified layout of the DCB doesn't affect the power module's switching behavior much if the module is operated under relatively low DC-link voltage and load current.

The turn-off / -on measurements, especially the turn-off under high load current, high DC-link voltage and high junction temperature, are also to be taken into account because the safe operating area of the power module is limited due to the module's internal stray inductances and other parameters. It is specified at the maximum temperature under switching conditions. This safe operating area is defined as "Reverse biased safe operating area", abbreviated as "RBSOA". In this area, with increasing currents, the allowed DC-link voltage is decreased. Furthermore, this derating strongly depends on system related parameters, like stray inductance of the DC-link and the current commutation slope during the switching transitions [39]. In order to check the operation of IGBTs at turn-off processes, the RBSOA test by maximum load current (2 x I_{CN} = 1600 A for HP2 module [85]) at the maximum temperature of 150°C are carried out on both sides of the half-bridge of the variant "Opt_Zero" module. In Fig. 6-5, there are two peaks in V_{CE}, as well as in V_{GE} of the IGBTs. The reason is that during the measurements Zener-diodes as clamping measure are used between auxiliary Collector and Gate to limit the voltage overshoot on the IGBT during its turn-off. The clamping diodes break through at about 650 V, in order to protect the IGBT. From the measurement curves it can be concluded that at maximum load current of 1600 A and maximum temperature of 150°C, the variant "Opt_Zero" shows similar RBSOA behavior as the one in the standard HP2. The only conspicuity is that the "Opt_Zero" show slight oscillation of V_{CE} and V_{GE} by the end phase of the turn-off process. The oscillation by LS is stronger than by HS. The root cause of these oscillations are investigated in this work; it has been found out that the changed current distribution in "Opt_Zero" module due to the modified DCB layout can cause local current circulation around some chips which contribute to the oscillations that are visible in Fig. 6-5.

The details of this phenomenon are explained through the following investigation regarding the current distribution of the modified DCB layout.

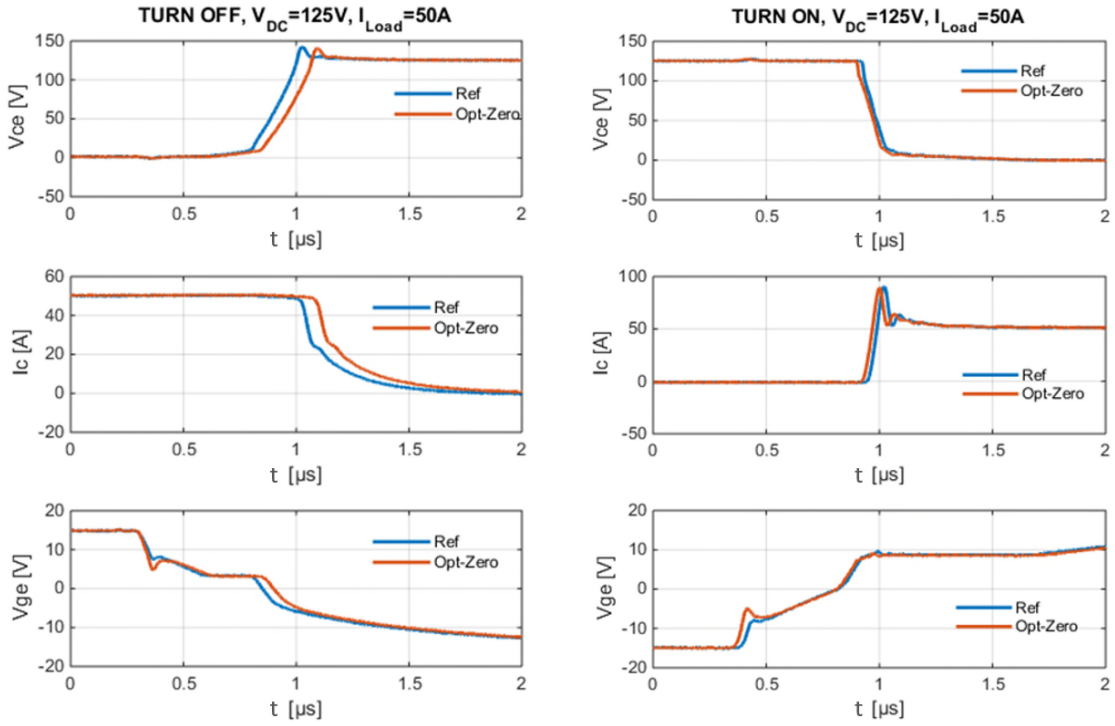


Fig. 6-4: Turn-off / -on tests at the same operation point as in EMI test in this dissertation (V_{DC} = 125 V, I_{Load} = 50 A, 25°C) for the comparison of "Opt_Zero" variant and standard HP2 module

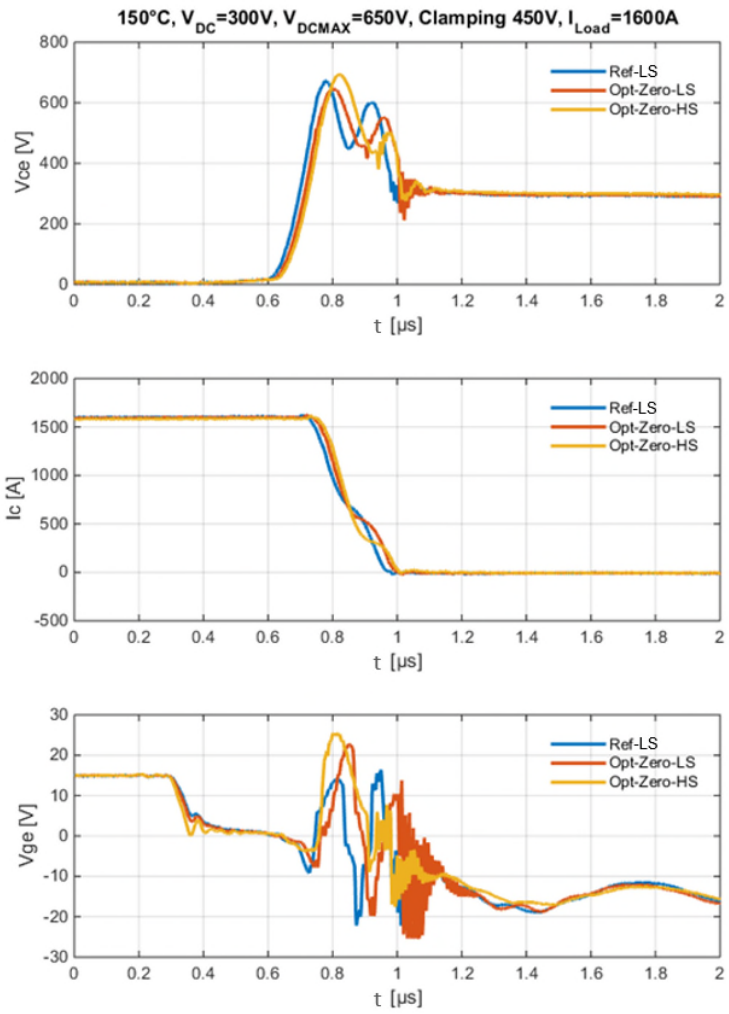


Fig. 6-5: RBSOA tests at maximum load current and temperature with clamping diodes for the comparison of "Opt_Zero" variant and standard HP2 module

As mentioned before, as the current distribution within the power module is changed because of the DCB layout modification, it is necessary to check if each chip is bearing different currents during the operation, especially when short circuit happens. The short circuit rating belongs to the essential characteristics of the power module and its semiconductors. It strongly depends on application specific parameters such as temperature, stray inductances, gate driving circuits and the resistance of the short circuit path. In this dissertation, a test setup as drawn in Fig. 6-6 is used. The IGBT in one side of the half-bridge is short circuited while the IGBT of the other side is driven with a single pulse. The corresponding voltage and current waveforms during the tests are illustrated in Fig. 6-7. The DC-link voltage is set up to 360 V to present the typical short circuit characteristics of the power module according to the datasheet [85]. The current I_{sum} (measured at the DC- terminal of the module) of the conducting IGBT increases rapidly with a slope which depends on parasitic inductances (including the metal bar in the test setup of Fig. 6-6). Within a defined short-circuit-withstand time of 6 µs the IGBT has to be switched off to avoid a device failure. Due to desaturation of the IGBT, the current should normally be limited to about 5 times the nominal current by the Infineon Trench/Fieldstop IGBT3 used in the module, while the collector-emitter voltage remains at the high level. However, because of the external stray inductance coming from metal bar, which takes over the most part of the voltage drop during the IGBT turn-on phase with big $\mathrm{d}i/\mathrm{d}t$, the collector-

emitter voltage drop of the IGBT cannot always remain at a high level. However, even if the DC-link voltage is set to be extremely low, there will always be voltage drop on the IGBT chips during the short circuit phase of 6 µs, basically because the IGBT chips are in desaturation status; the low DC-link voltage stimulates less di/dt, thus the inductive voltage dip will be proportionally much less, even invisible.

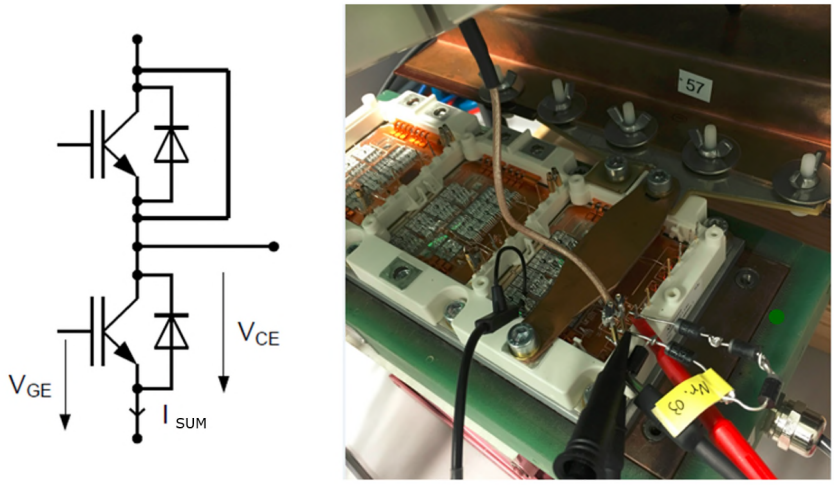


Fig. 6-6: Short circuit test setup in wiring diagram (left) and in laboratory building with clamping diodes (right)

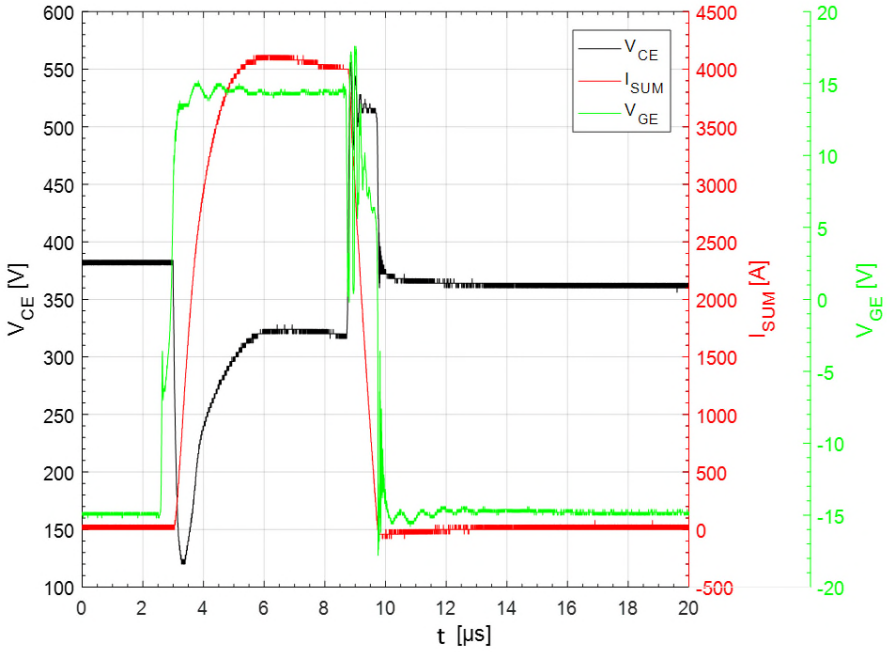


Fig. 6-7: Voltage and current waveforms during the short circuit tests for HS IGBT at 60°C: black for V_{CE}, red for I_{sum}, green for V_{GE} in power module "Opt-Zero"

By checking the current distribution of different points in "Opt_Zero", the currents flowing on four different positions on each side of the half-bridge (A to D shown in the figures) are measured at 60°C for comparison. The results are shown in Fig. 6-8 and Fig. 6-9. For the flowing currents of each measurement point there is only half of the bond wires of each IGBT (or diode) chip been captured. Visibly, for the HS chips the currents are distributed similarly

within A to D points. For the LS chips, the current of D behaves in a way much different from the rest of the points. At point D, the current reduces itself extremely quickly during the switch off process of the IGBTs. That indicates the chip at point D acts more quickly than the other three chips. The explanation for that is divided into two parts:

On one hand, as mentioned in 6.1.1 for the IGBT at point D, because it is located nearest to the LS gate pin and auxiliary emitter pin, the stray inductances and resistances in its gate-emitter loops are smaller than at other points (A to C), even if the etching trench ① in Fig. 6-3 is specially designed to weaken this unbalance. The etching trench can help to rebalance the resistances of each gate-emitter loop of A to D, however, the stray inductances of each loop are mostly affected by the spacing between the IGBT's gate-pad and the module's auxiliary emitter pin. So, the extra added etching trench on DCB wouldn't help much to symmetrize the stray inductances. That makes the chip D act more quickly than the other chips when the gate signal comes.

On the other hand, in the measurements points A to D of both sides of the half-bridge, the currents don't fall to zero immediately after the IGBT turn-off process. Especially for LS, the tail currents can be observed in Fig. 6-9, flowing in positive and negative directions dependent on the concrete measurement positions. That indicates, after the turn-off of the IGBTs, there are still short-term currents flowing through the measured bond wires. Such short-term currents are caused by the stray inductances of DCB copper layer which are marked in yellow in the figures. During the IGBTs switching off, by carrying the short circuit current I_{SUM} with large $\mathrm{di/dt}$, the copper layers can induce voltage drop on themselves, forming local current circulation around each chip surface area (black loops in the figures). Each loop consists of three parts: the DCB copper layer, the bond wires, and the chip front side metallization. The amplitude of each induced voltage depends strongly on the chip position in the module layout. The current density increases when it gets close to the module terminal. For example, in Fig. 6-9, from position A to D, the current from each chip adds up on the copper layer, flowing towards the DC- terminal. That makes the $\mathrm{di/dt}$ increase progressively from A to D. The induced voltage at the location D is therefore the largest; it inspires the largest local current of approx. 200 A to circulate around as long as the $\mathrm{di/dt}$ of I_{SUM} exists. After I_{SUM} reduces to 0 A, the circulating current also attenuates to zero within a few micro seconds. Knowing from the measurement that the $\mathrm{di/dt}$ of I_{SUM} during IGBT turn-off is 4.4 kA/µs, the resistance of the parallel bond wires in the local loop amount to 1 mΩ (for Al bond with diameter of 400 µm, with circumference of approx. 10 mm for the loop), the induced voltage V_{ind} must be at least 200 mV to inspire the circulating current of 200 A. The stray inductance of the DCB copper layer can therefore be calculated by using $L_s = V_{ind}/\frac{di}{dt}$. It amounts to 45 pH. The conspicuous current peak at the location D during the IGBT turn-on in Fig. 6-9 can also be explained in a similar way, whereby the $\mathrm{di/dt}$ during I_{SUM} increment induces the voltage drop from the opposite direction. The circulating current thus adds up with the short circuit current of the chip at D position and forms a peak of approx. 1200 A. For the module HS the circulating currents work also according to the same principle, except for position A (Fig. 6-8). Due to its special position near to the AC terminal of the module, the short circuit current I_{SUM} cannot induce voltage at A area, so there is no tail current that can be measured.

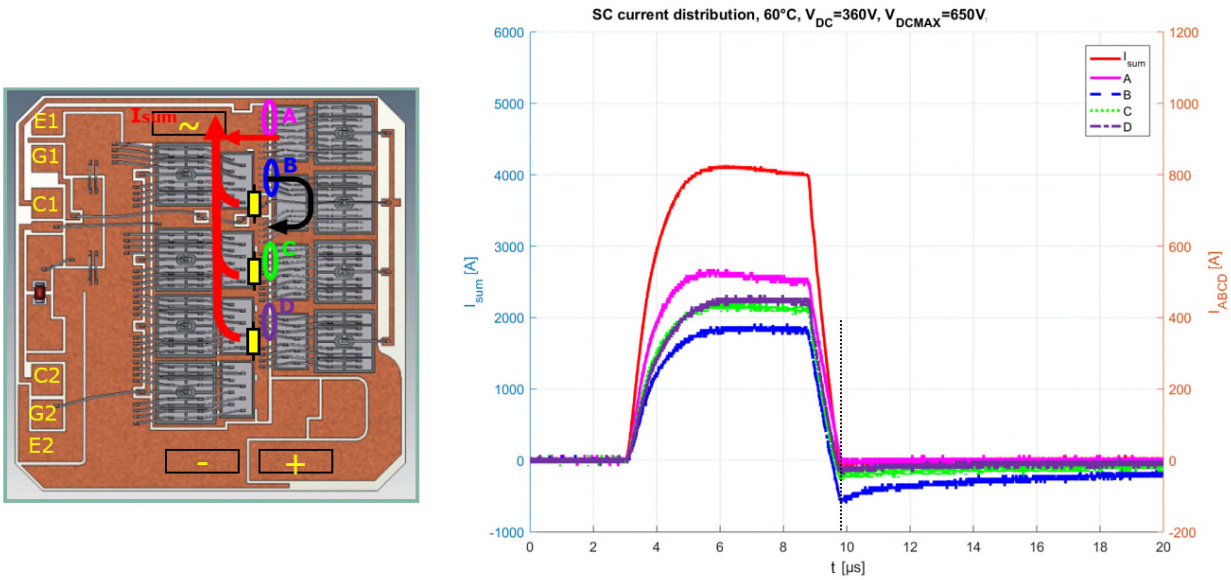


Fig. 6-8: Checking the current distribution of HS IGBTs in "Opt_Zero" by short circuit test

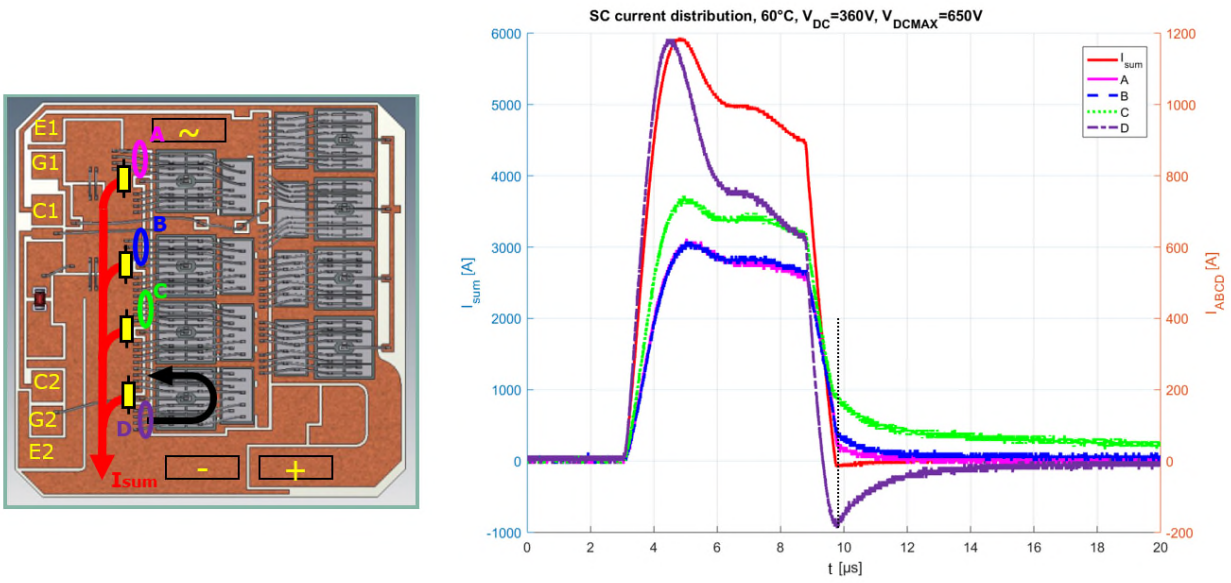


Fig. 6-9: Checking the current distribution of LS IGBTs in "Opt_Zero" by short circuit test

By using the setup for the conventional EMI measurement by a buck-converter operation that has been explained in chapter 4.1 and 3.2, the EMI behavior of the variant "Opt_Zero" is presented in Fig. 6-10 to compare with the standard HP2 module. It can be seen from the measurement result, that in the frequency area from 150 kHz to 108 MHz [67], normally classified for conducted emissions in automotive applications, the EMI optimized DCB layout (summarized as Concept 1 in Fig. 6-1) has brought only a small improvement of the EMI performance: the "Opt_Zero" module brings attenuation of 2 to 5 dBµV in HF (High Frequency) area; because of the symmetry of DC+ and DC- sides, a resonance point of standard HP2 around 45 MHz in VHF (Very High Frequency) ranges has also been eliminated in "Opt_Zero" module.

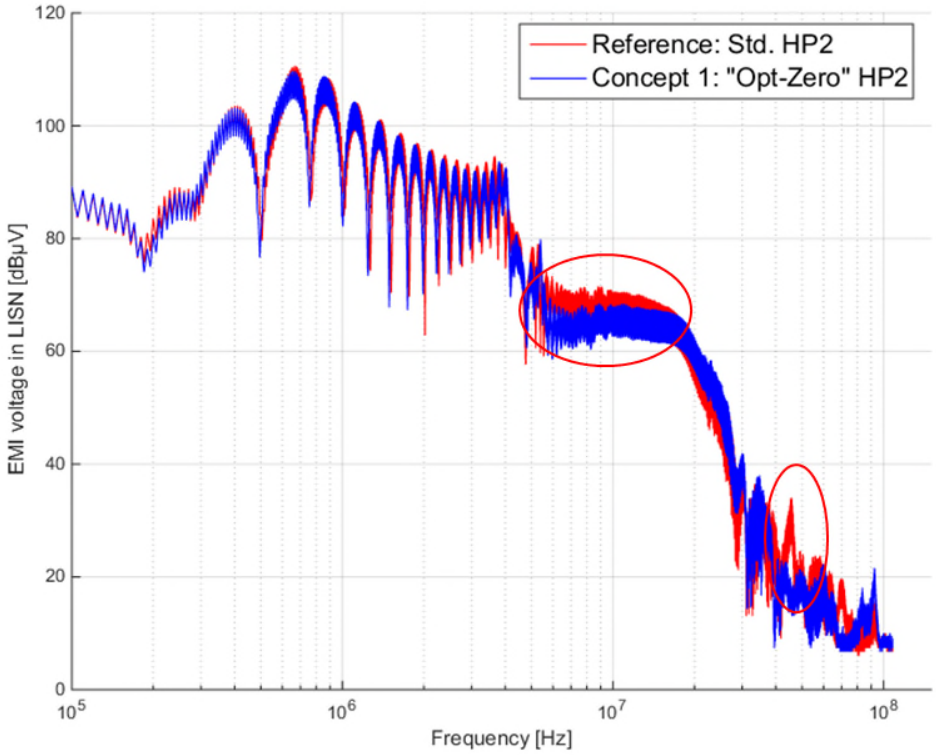


Fig. 6-10: Comparison of the conducted EMI spectrum (in average) between the standard HP2 and the variant power module "Opt_Zero", at V_{DC}=125 V, I_{RMS_Load}=50 A, f_{switch}=10 kHz

6.2. Reducing the DM interference by integrating X-Capacitors into the power module

Since the DCB layout changing has not brought about a significant improvement of the power module's EMI performance, there have to be further measures to continue the optimization. According to the spreading mechanisms of the interferences presented in 2.1.2, the disturbances that have been created during the switching of the semiconductors can flow in the loop consisting of the halfbridge of the power module, the DC-link and the connection between them. This loop is usually named commutation cell of the HV system. Due to the parasitc capacitances and the stray inductances of the commutation cell itself, the currents that flow in the cell can cause resonances and further lead to interference peaks in the EMI spectrum [54]. The origin of such resonance has already been discussed in 5.2. In this dissertation, to suppress such resonance and reduce the EMI, some capacitors are chosen to be integrated directly into the power modules. For the DC-link voltage of about 300 V, the capacitors for interference suppression in power electronics applications usually have capacitance values between 10 nF and 5 µF [6]. In cooperation with EPCOS®, an innovative component "CeraLink™ capacitor for fast-switching semiconductors" has been defined , with the capacity of 1 µF and 5 µF as well as relatively low ESL and ESR. According to the datesheets in [87] and [88], the typical electrical characteristics and electrical ratings of the CeraLink™ capacitors are summarized in Table 10 and Table 11.

The specification of the components ensures them to be assembled in the power module for the study of the EMI improvement potential, which is actually the purpose of this dissertation. Since the components currently do not meet the temperature requirements of a power electronics product necessary for productive use, there are no statements avaliable with respect to the lifetime and the load limits for this proposal. However, the constructive feasibility of this proposal in building of prototype has been verified and implemented within this dissertation. Fig. 6-11 shows the direct soldering of the capacitors onto the DCB of a standard HP2 power module. Through the measurement results in Fig. 6-12 it can be seen that the EMI performance of the module after the integration of the capacitors is improved in certain frequency ranges by approx. 6 to 10 dBµV reduction of the emissions in the frequency range from 6 to 25 MHz. Besides, it can also be detected that the integration of the capacitors of 1 µF or of 5 µF show similar effects. These measurement results are in good agreement with the simulation results with regard to the differential-mode of the EMI in chapter 4.2.1. There, it is predicted that the X-capacitors will lead to a damping of the DM interference of 6 to 10 dBµV in the frequency range from 2 to 20 MHz. The additional higher spectrum peaks due to the series resonances (see Fig. 4-8 right) are covered and invisible in the measurement results because of the dominance of the common-mode interference in most frequency ranges. In the lower frequency ranges up to about 7 MHz, the CM interference is much greater than the DM interference, which explains why the attenuations as well as the resonance in the DM interference of 2 to 7 MHz can not be recognized after the integration of the X-capacitors. From about 7 MHz onwards, the DM interference is dominating again, so that the effect of the X-capacitors in the spectrum can be seen up to approx. 25 MHz. From 25 MHz to approx. 41 MHz, the DM interference is still in the dominant position, however, there is no more reduction of the interference in the measured spectrum to be recognized, since the X-capacitors are no longer effective in this frequency range due to their own ESL.

Table 10: Typical electrical characteristics and electrical ratings of CeraLink™ capacitor of 1 µF, 500 V

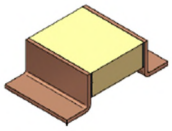
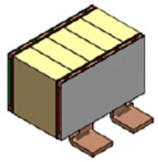
	ESR 0 V_{DC}, 0.5 V_{RMS}, 25 °C, 1 MHz	**ESR** 0 V_{DC}, 0.5 V_{RMS}, 25 °C, 1 kHz	**ESL**	**I_{op} [1)]** 100 kHz T_A = 85 °C	**I_{op} [1)]** 100 kHz T_A = 105 °C
	**mΩ**	**Ω**	**nH**	**A_{RMS}**	**A_{RMS}**
	12	3.3	2.5	7.5	5.2
1µF, 500V	[1)] Normal operating current without forced cooling at T_{device} = 125°C. Higher values permissible at reduced life time.				

Table 11: Typical electrical characteristics and electrical ratings of CeraLink™ capacitor of 5 µF, 400 V

	ESR 25°C, 100kHz	**ESL**	**$I_{ripple,op}$ [1)]** 100kHz	**$I_{ripple,max}$ [2)]** 100kHz
	**mΩ**	**nH**	**A_{RMS}**	**A_{RMS}**
	5	4.5	6	10
5µF, 400V	[1)] continuous operation mode (OT ≤ 40°C, T_{device} ≤ 125°C) [2)] reduced operation time (OT ≤ 60°C, 125°C ≤ T_{device} ≤ 150°C)			

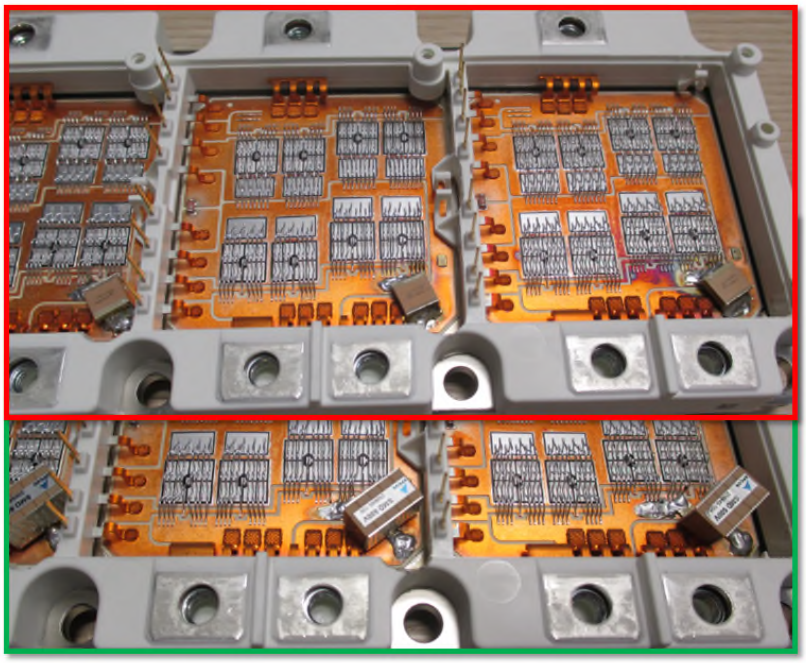


Fig. 6-11: Mounting of the CeraLink^{TM} capacitors of 1µF (red) and 5µF (green) as X-capacitors directly in the standard HP2 power modules

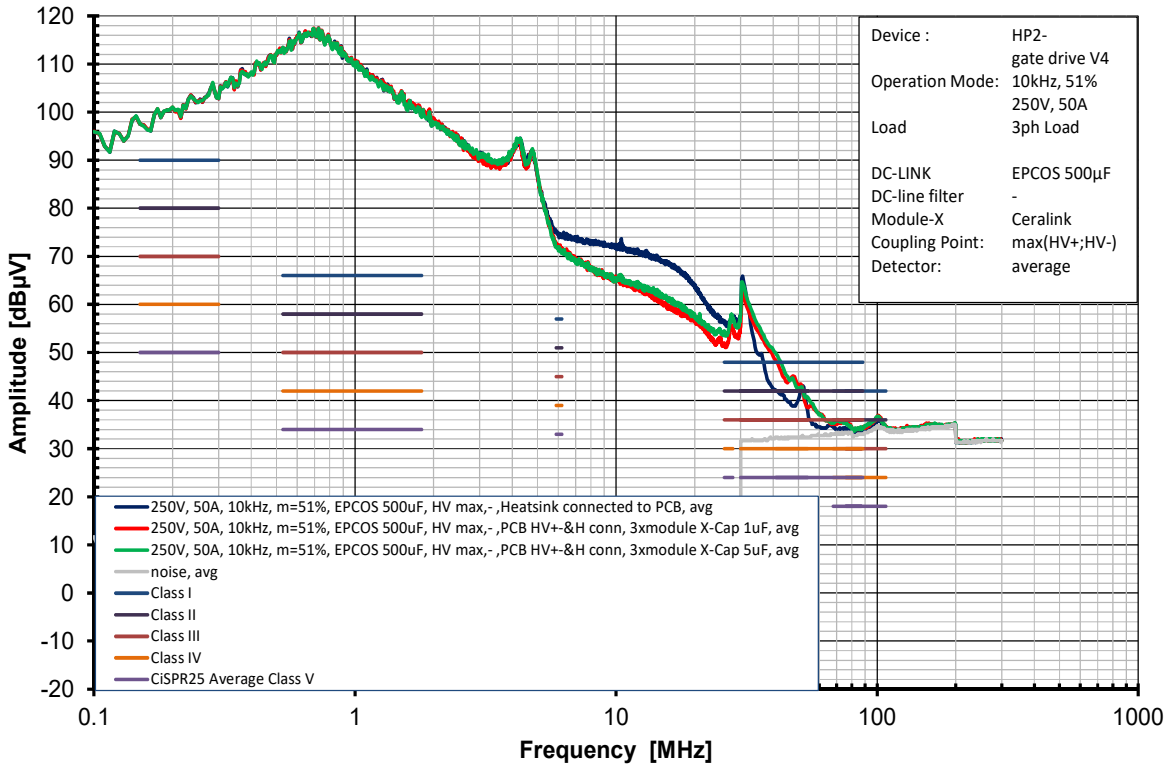


Fig. 6-12: Reducing the EMI of standard HP2 in certain frequency range (6 to 25MHz) due to integration of X-capacitors of 1µF (red) and 5µF (green)

Compared to the standard HP2 DCB layout, it is much easier to integrate the X-capacitors onto the DCB of the “Opt_Zero” variant. As discussed in chapter 6.1.1, an island-like area marked as ② in Fig. 6-3 is designed for the “Opt_Zero” layout, so that there will be enough space reserved for the mounting of a capacitor as well as some snubbers later. In Fig. 6-13 the power

module variants with / without X-capacitors are presented and compared. "Opt_Zero" is the realization of the above-mentioned concept 1. The second variant "Opt_X_1µ", created by additional mounting of the X-capacitor (of 1µF) into the module, can be counted as a combined solution of the concepts 1 and 2. The new variant with X-capacitors has also been electrically characterized through the same measurements used for “Opt_Zero”; its EMI performance is compared with the standard HP2 as well as “Opt_Zero” HP2. The simplified circuit diagram in Fig. 6-13 illustrates where the voltage and current are measured during the characterization. For the variant "Opt_X_1µ", the current I_{Module}, which is measured at the terminal of the power module, is actually a combination of the chip current and the X-capacitor current. Fig. 6-14 shows the signal delay during the switching on and off of the IGBTs for the "Opt_" variants, since the bonding wires to the gate (for HS switches) and the DCB copper track to the auxiliary emitter (for LS switches) are much longer than those of the reference module due to the new substrate design. It can be noticed that by IGBT turn-off process, the overvoltage peak of variant “Ref” as well as “Opt_Zero”, which not only contributes to the EMI, but also limits the blocking voltage of the power module, has been considerably reduced due to using the X-capacitor in the variant "Opt_X_1µ". The oscillation with the period of approx. 2 MHz in the load currents of “Opt_X_1µ” can be observed because the X-capacitors causes a new resonance loop between the capacitor and the DC-link through the module terminals. Through extra measurements in [82], which split the X-capacitor current out of the total terminal current, it can be found out that this oscillation does not significantly affect the chips. Additional losses on chips during the switching are not observed. By using the measurement method introduced in [82], in Fig. 6-15 the switching losses E_{sum} (sum of turn-on loss and turn-off loss) of the variants “Opt_Zero” and “Opt_X_1µ” are compared to the standard module “Ref”, in which only the current flowing through the chips is counted. The load currents of the power module are varied from 50 A to 400 A so that the switching losses can be compared under different working points. Through the measurement results it can be seen, the switching losses of the three variants remain almost the same when the load current grows. The switching losses of the two modules without X-capacitors are also comparable. However, from the system’s aspect, the energy dissipated in the X-capacitors due to its ESR (e.g. heat loss) comes originally out of the power source of the system. So, in the electrical drive system of a vehicle, this will cause extra burden of the HV-battery.

On the other hand, from the EMI’s aspect, the use of X-capacitors directly in power module has indeed brought benefits. Fig. 6-16 shows the measured conducted interference spectra of the new variant (in green) compared to the standard HP2 as reference (in red). The primary variant “Opt_Zero” (in blue) has also been put in the same place for the comparison. The modification of the DCB layout according to concept 1, in combination with the use of the X-capacitor according to concept 2, results in not only an attenuation (5 to 15 dB) in the range of 6 MHz to 25 MHz, but also the deterioration of the performance (5 to 10 dB) around 30 MHz. The deterioration is caused by a newly formed LC resonance after the X-capacitor insertion. As mentioned in chapter 5.2, the differential mode resonance loop usually consists of the DC-link, the HS or LS chip which is in blocking state in the half-bridge, and the stray inductances lying between them. When X-capacitor is integrated into the module, a new DM loop is formed, consisting of the X-capacitor itself, the capacitance of HS or LS blocking chip, and the power module’s stray inductance. In “Opt_X_1µ”, the module stray inductance of 14 nH, the ESL of the X-capacitor of 2.5 nH (see Table 10) as well as the chip capacitance of 1.5 nF (see Table 7) together build up a LC loop with a resonance frequency of 32 MHz. The capacitance of X-

capacitor itself can be neglected in this new DM loop, since it is in a series connection with the chip capacitance, which is much smaller than 1 µF. By comparing the measurement results from Fig. 6-12 and Fig. 6-16 , the following conclusions can be drawn:

- Integrating the X-capacitors in the range of 1 µF to 5 µF directly in power module can bring about the evident attenuation of the conducted EMI in the range of about 6 MHz to 25 MHz;
- The effect of the attenuation can be reinforced by about 5 dB, if the DCB layout of the power module is symmetrized regarding its parasitic capacitances and stray inductances of DC+/- sides;
- There are also frequency areas (about 30 MHz to 50 MHz), in which an unexpected increase of the conducted EMI of 5 to 10 dB can be observed.

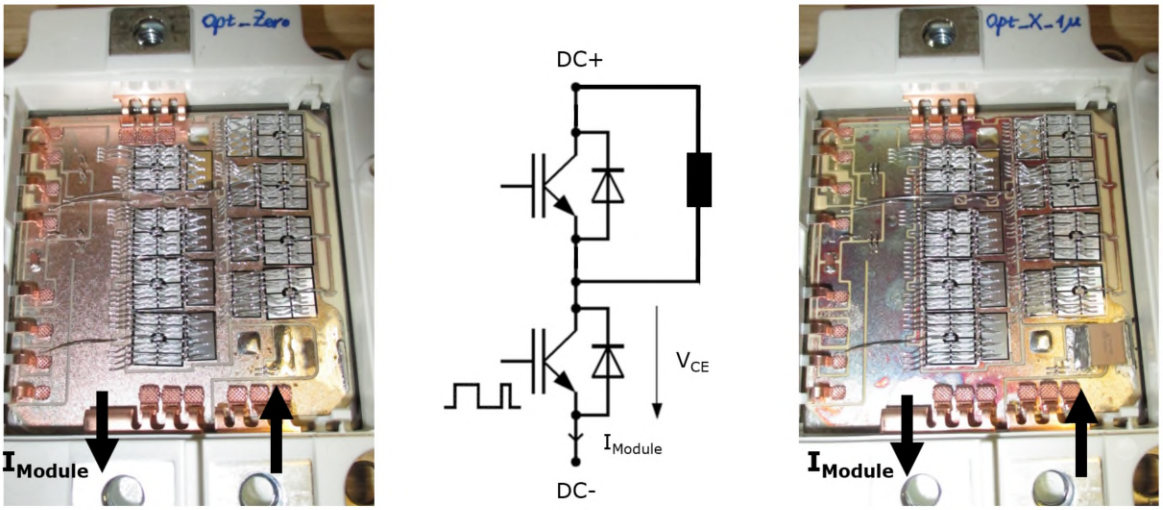


Fig. 6-13: Opt_HP2 module variants group 1: “Opt_Zero” (left) and “Opt_X_1µ” (right)

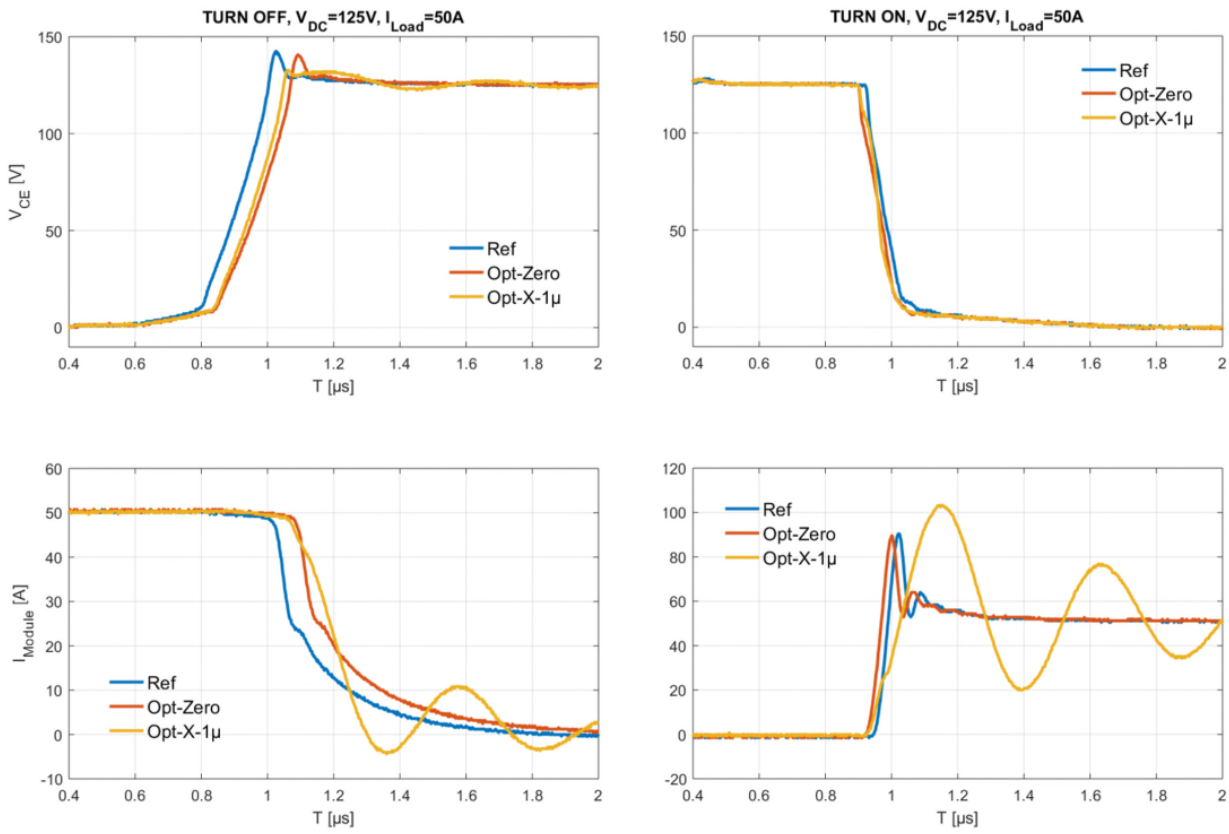


Fig. 6-14: Comparing the switching behavior of the variants group 1: "Opt_Zero" (red) and "Opt_X_1µ" (orange) to the standard HP2 as reference (blue)

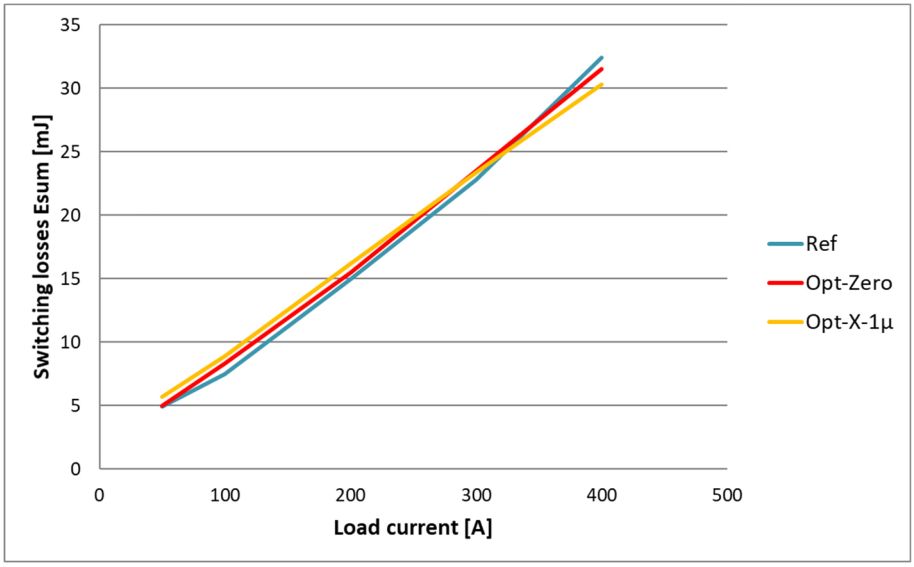


Fig. 6-15: Comparing the switching losses of the reference and variants with or without using the X-capacitors (Tj = 25°C)

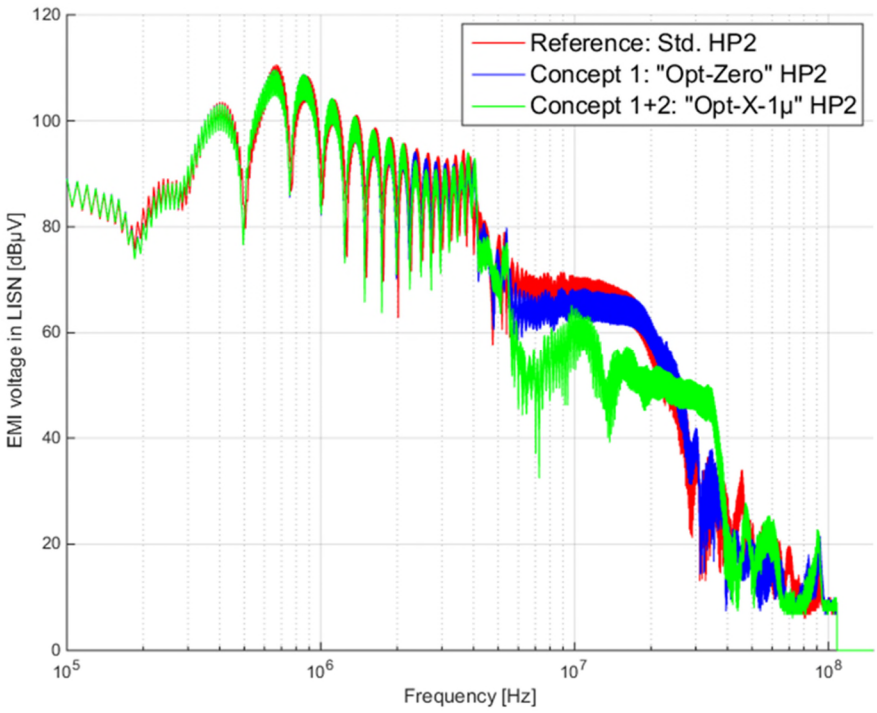


Fig. 6-16: Comparison of the conducted EMI spectrum (in average) between the standard HP2 and the variants power module "Opt_Zero" as well as "Opt_X_1µ", at V_{DC}=125V, I_{RMS_Load}=50A, f_{switch}=10kHz

To extend the research regarding the use of the X-capacitors in power module, more prototypes are built up for the tests in this dissertation. Besides the CeraLink™ capacitors from EPCOS®, the bare-die-shaped snubbers produced by Fraunhofer IISB are selected. This type of monolithic RC-snubber up to 600 V, according to the datasheet from IISB [89], is formed by a deep trench in silicon filled with SiO_2 or Si_3N_4 as dielectric and doped poly-silicon as electrode. The bulk silicon can be used to form the series resistor of a passive RC-snubber. The bottom side contact consists of a solder- and sinterable metal stack. The top side contact consists of bondable aluminum, or is solder- and sinterable on request. These characteristics make it suitable for the integration into the power module directly, since during the power module construction, the snubber can be mounted the same way as the semiconductor bare-dies, especially by the chip soldering process and the wire bonding process. In addition, the spread of the thermal power dissipation to the heat-sink of the power module is also more efficient.

By using the snubbers from IISB and the CeraLink™ capacitors from EPCOS, the solution for optimizing the EMI performance of the power module can be realized by combining the before mentioned concept 1, 2 and 3. Parallel to the modules in Fig. 6-13, the second group of prototypes is built up and shown in Fig. 6-17. The series "Opt_S" represent the modules, which are equipped with the IISB snubbers (5.5 nF / 1.6 Ω or 20 nF / 0.5 Ω). It was found that only the size of the 5.5 nF type snubber fits into the modified DCB layout. In contrast to typical snubbers, which are parallel to the semiconductor chips, the 20 nF type can only be arranged as an X-capacitor (marked as "Opt_XS_20n5n5") between DC+ and DC- because of the limited space available next to HS and LS chips. In the case of the collector-emitter cut-off current or break down voltage measurement of the power modules, it should be noted that the snubbers can break through at approx. 500 V to 600 V, ealier than the IGBT and diode chips. Besides, this kind of measurements shall be carried out with continued DC voltage and not as

usual under pulse voltage with gradually increased amplitude, since the snubbers under pulse voltage will stay in the status of charging and discharging, that can falstify the measurement result of I_{CES}. Regarding the switching behavior, with the measurement results from Fig. 6-14 combined, it can be found out from the compiled curves in Fig. 6-18 that there are no major differences between the five "Opt_" variants. The use of the bare-die-shaped snubber (of 5.5 nF / 1.6 Ω) according to the concept 3 shows no substantial change of the switching curves. The use of the X-capacitor still brings about additional oscillation in the load currents, even if it is combined with the snubber. The period of the oscillation depends on the capacitances: The X-capacitor of 1µF produces an oscillation of approx. 2.5 MHz; By 500 nF the frequncy of the oscillation is increased to approx. 3.3 MHz. The attenuation of such oscillations is possible, if one connects a resistor in series to the X-capacitor. Howerver, the connection between the resistor and the DCB has to be reliable to conduct large AC current (> 100 A), so a SMD formed resistor cannot be taken into account. Using a large resistor will cost extra place, which turns to be unrealistic by the existing DCB layout in this work. Therefor, the proposal is not followed further, as long as no special effects can be detected in the EMI spectra.

The EMI spectra of the three "Opt_S / XS" variants compared to the reference module are shown in Fig. 6-19. The following conclusions regarding the combination of concepts 1 + 2 + 3 can be derived from it:

- The integration of RC snubbers parallel to IGBT does not bring significant benefit;
- "Opt_XS_500n_5n5" is the best variant for > 10MHz, but it shows a high resonance at 230 kHz. If this resonance is regarded as problematic for the application, the variant "Opt_XS_20n_5n5" would be the alternative approach of the solution;
- All variants show a significant improvement of the EMI attenuation around 25 MHz to 35 MHz.

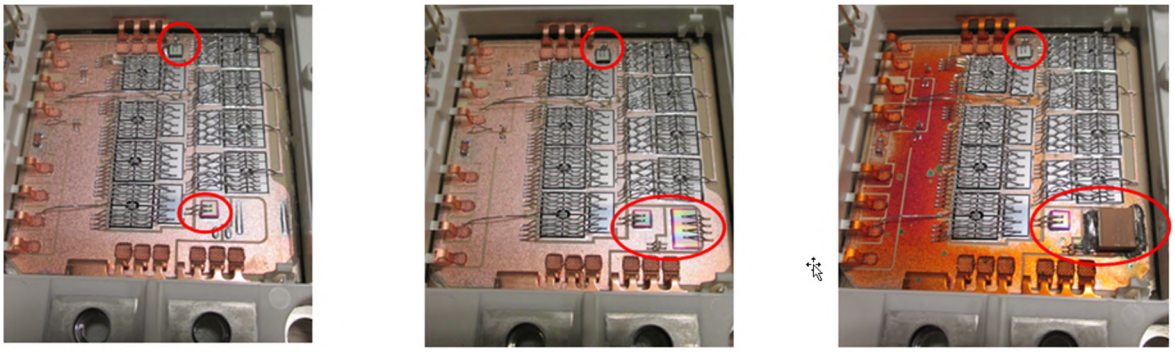


Fig. 6-17: Opt_HP2 module variants part 2: “Opt_S_5n5” (left), “Opt_XS_20n5n5” (medium) and “Opt_XS_500n5n5” (right)

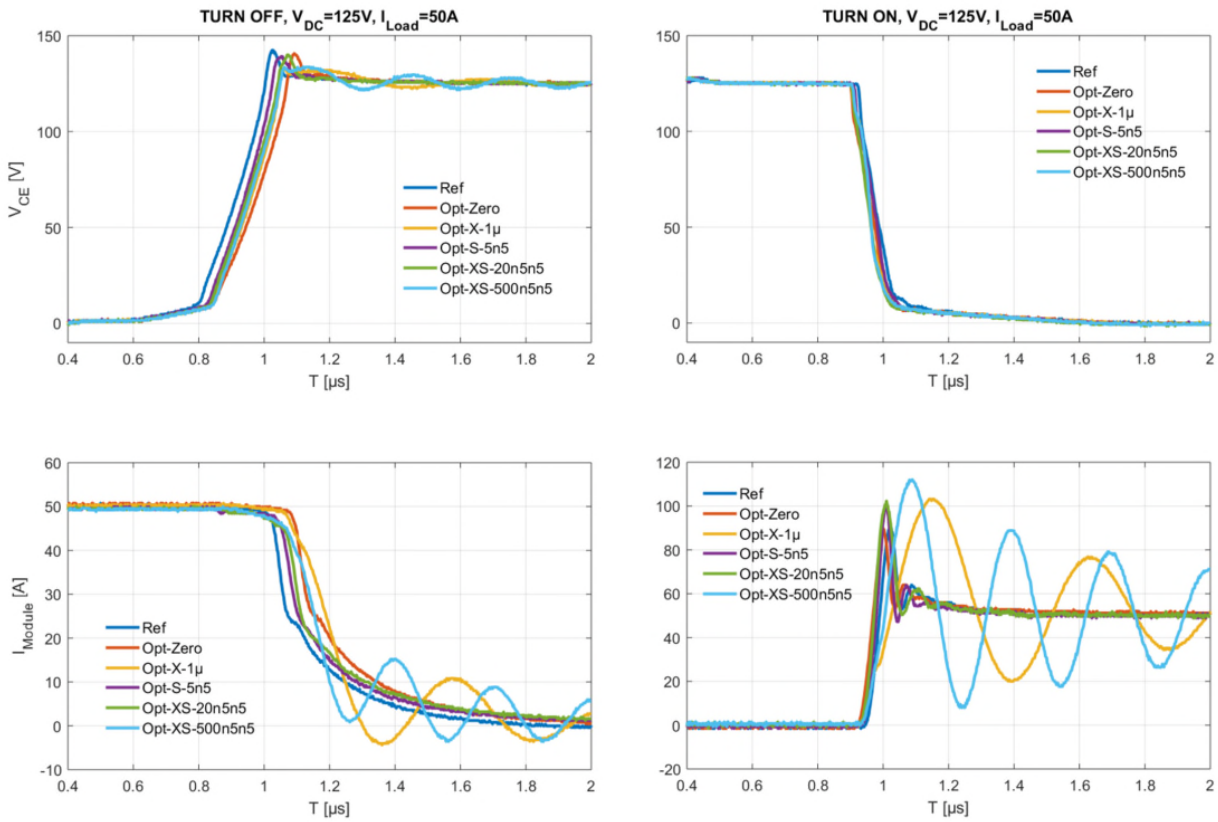


Fig. 6-18: Comparing the switching behavior of the variants group 1 (“Opt_Zero”, “Opt_X_1µ”) and group 2 (“Opt_S_5n5”, “Opt_XS_20n5n5”, “Opt_XS_500n5n5”)

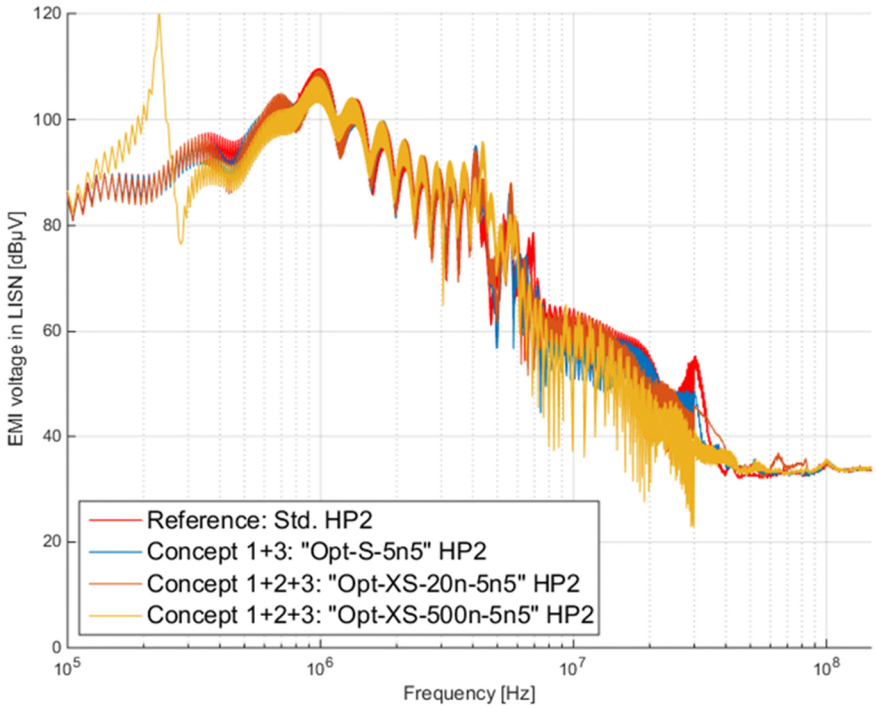


Fig. 6-19: Comparison of the conducted EMI spectrum (in average) between the standard HP2 and the variants power module “Opt_S_5n5”, “Opt_XS_20n_5n5” and “Opt_XS_500n_5n5”, at V_{DC}=250V, I_{RMS_Load}=50A, f_{switch}=10kHz

6.3. Reducing the CM interference by integrating Y-capacitors into the power module

Through the simulative analysis in chapter 4.2.1 and the experimental approach in chapter 6.2, it can be confirmed that the conducted EMI in differential mode is not dominating in the relevant frequency range from 100 kHz to 108 MHz [67]. In this dissertation, in order to achieve even better attenuation effects, the use of Y-capacitors due to the spreading mechanism of the CM conducted EMI is also taken into account. As mentioned in chapter 2.1.2, the Y-capacitors are widely used as CM filter in drive systems of industrial and automotive applications, because they can create a low impedance path for CM conducted interference at the DC side of the inverter to ground. From the power module's aspect, there are two options available for the realization. One option is the soldering of the CeraLink™ capacitors to the driver board of the power module (via special PCB connections from DC + / - to ground). In this way, the capacitors can be integrated relatively easily without modifying the power module itself. However, due to the relatively large distance between the interference source and the Y-capacitors, an additional stray inductance of approx. 50 nH is brought along into the loop, which reduces the effect of the capacitors. In the measurement, this approach has not only resulted in the attenuation of the conducted EMI in the MF range, but also induced a new resonance peak at about 2 MHz.

The alternative is to install the CeraLink™ capacitors directly in the power module. For this approach, several cuttings on the power module frame are necessary in order to provide sufficient space for the capacitors' connection between DC+/- and the module substrate. In this way, the capacitors, which fulfill the Y-filter function to attenuate the CM interferences, can be connected to the power module with extremely low ESL. Compared to the use of capacitors on driver boards, this approach shows not only the attenuation in the MF range, but also better performance in the 7 to 40 MHz range. To realize this approach in this work, the problems during prototyping need to be noticed: Firstly, since the module frame has been damaged previously, the prototype can no longer be tested in the special isolation-voltage test for safety reason. Secondly, since the sealing between the frame and the baseplate is damaged because of the insertion of the Y-capacitors, the silicone gels of the module meant to protect the power chips from harsh environmental conditions (moisture, in particular) and to provide electrical insulation for high voltage operations, are no longer suitable for the prototype during the manufacture. This will possibly lead to a reduction of the module reliability. However, the aforementioned problems can be avoided if the module frame is redesigned and its sealing to the baseplate is adjusted. By doing that, the module can then be used for the productive purpose.

To implement the Y-capacitor concept without breaking the power module frame, the changed DCB-layout "Opt_Zero" is more suitable for use, since by this customized layout there are more spaces previously reserved for the installation of the capacitors between the HV-system and the module substrate. Fig. 6-20 shows the last part of the prototypes that is built up in this dissertation. All variants of this part are respecting the realization of the combination of the before mentioned concepts 1 and 4/4*. By using the CeraLink™ capacitors of 250 nF as Y-capacitors, the isolation class of the power module is reduced from 2.5 kV to 900 V. Due to the vehicle test requirement of the car manufacturer (BMW AG in this dissertation), the isolation

class of the module must be no less than 2 kV for safety reasons in the vehicle. Therefore, the integration of foil or ceramic capacitors with Y2 voltage class was carried out after processing the module frames. These prototypes are identified as "Opt_Y2F" and "Opt_Y2K" (“F” for foil, “K” for ceramic). Due to the spatial limitation, the installation of the capacitors with Y2 voltage class is only possible up to the type of 10 nF.

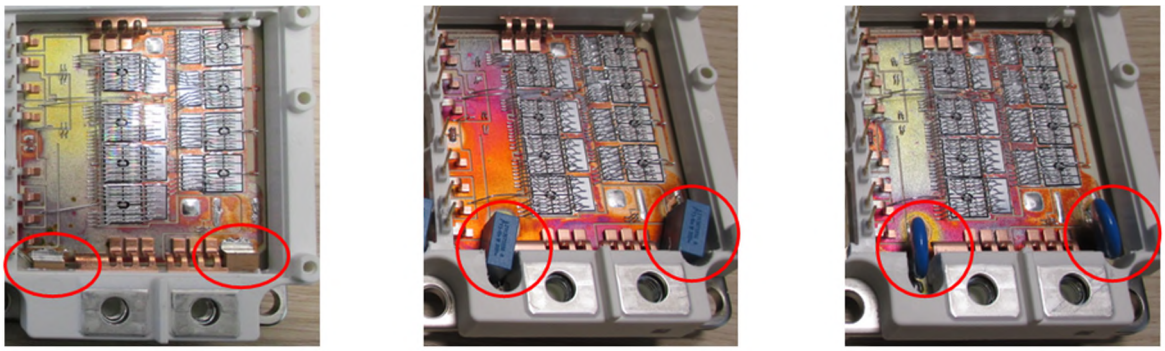


Fig. 6-20: Opt_HP2 module variants part 3: “Opt_Y_250n” (left), “Opt_Y2F_10n” (center) and “Opt_Y2K_10n” (right)

The switching behaviors of the prototypes with Y-capacitor, as shown in Fig. 6-21, don’t show any significant differences between each other. Compared with the standard HP2 as a reference, the use of the Y-capacitors also leads to oscillation in the load currents, since they are series-connected through the module substrate and thus also work at the same time as X-capacitors between DC+ and DC-. The periods of the oscillations are dependent on the capacitances: the 250 nF Y-capacitor causes an oscillation of approx. 5.4 MHz; Using the foil or ceramic capacitors of 10 nF with Y2 voltage class produces expected oscillations in higher frequency range at approximately 11.1 MHz. These oscillations are transformed into the peaks of the EMI spectra, which can be clearly seen in Fig. 6-22 and Fig. 6-23. With regard to the additional peaks in the spectra caused by the installation of the Y- / Y2-capacitors in power modules, the amplifying of the interferences in certain frequency ranges can be explained by using the resonance-mechanisms of the CM- and DM-networks that are presented by the “passive measurement” in chapter 5.1 and 5.2. Briefly speaking, the newly occurring resonances in the spectra after the installation of Y- / Y2-capacitors can be explained with series LC resonant circuits respectively caused by the C’s and the ESL’s of the Y- / Y2-capacitors and the other system components within the impedance network. For example, the oscillation of approx. 5.4 MHz by the variant “Opt_Y_250n” is caused by a LC resonance loop with L = 25 nH and C = 35 nF: This loop consists of the both Y-capacitors (for DC+ and DC-), their ESLs, the DC-link and the module DC terminal stray inductance between them. According to the characteristic of the CeraLink^{TM} capacitors of 250 nF in [87], the capacitance is proportional to the operation DC voltage. At room temperature, at the voltage of 125 V in DC-link (62.5 V for each Y-capacitor), the capacitance is approx. 54% of the typical effective capacitance of 130 nF, which is approx. 35 nF for two Y-capacitors in series connection through the module baseplate. The ESL from the DC-link (15 nH) as well as from the two Y-capacitors themselves (2 x 2.5 nH) and the stray inductance of the module’s DC terminals (approx. 5 nH) together contribute to the L of 25 nH. The oscillation of approx. 5.4 MHz is so formed.

This explanation matches also the modeling and the measurement results in [40], where after using the Y-capacitors outside of the power modules, the origin of the multiple peaks in the

EMI spectra are discussed. The origin of the other peaks in Fig. 6-22 can also be explained in a similar way: The first peak of 0.14 MHz is caused by the CM resonance loop consisting of the two Y-capacitors in parallel connection to GND and the two inductances of 5 µH in the LISN (2.5 µH). The second peak of 3 MHz is caused by another CM resonance loop which consists of a series connection of the following components: the two Y-capacitors, the load capacitance (approx. 6.6 nF, see chapter 4.2.1), the inductance of the motor wires (400 nH) and the ground strap (approx. 20 nH, see 4.1.2). In this dissertation, since the main purpose of the research is to realize concepts of EMI optimization at power module level and evaluate them afterwards, the further modeling and simulation for investigating the multiple peaks in the spectra are therefore omitted.

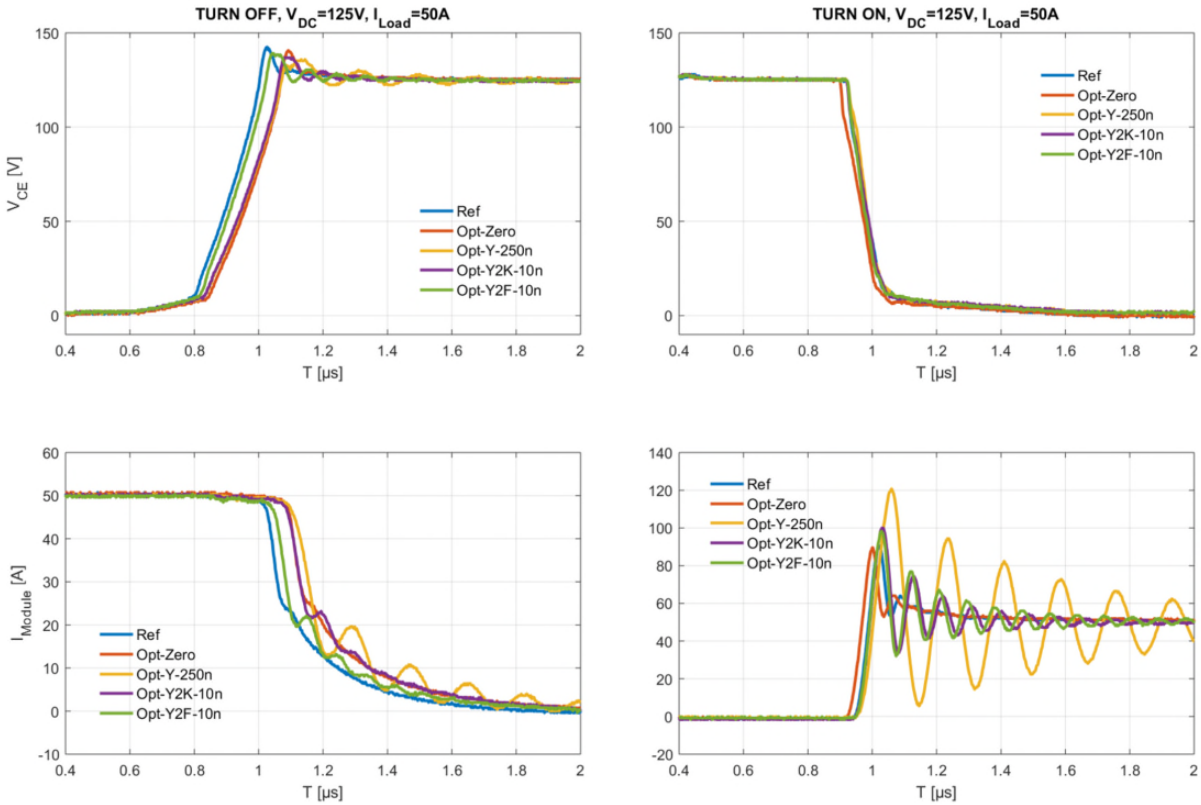


Fig. 6-21: Comparing the switching behavior of the variants group 3 (“Opt_Y_250n”, “Opt_Y2F_10n” and “Opt_Y2K_10n”)

The conducted EMI spectra of these five "Opt_Y / Y2" prototypes are compared with the reference HP2 module as before. The following statements regarding the EMI optimization concepts “1 + 4 / 4*” can be derived from this:

- "Opt_Y_250n" is the best of all variants for > 200 kHz. Except the two additional resonance points at approx. 3 MHz and 5.4 MHz, the variant shows up to 30 dBµV attenuations in MF and HF frequency ranges;
- "Opt_Y2F_10n" and "Opt_Y2K_10n" show nearly identical interference spectra up to 60 MHz. The capacitive value therefore plays a larger role than the capacitive material

in this frequency range does. The two versions also show good attenuation effects up to 20 dBµV in MF and HF frequency ranges;

- The use of the Y capacitors according to concepts 1 + 4 / 4* shows a much stronger EMI optimization effect than the other approaches do.

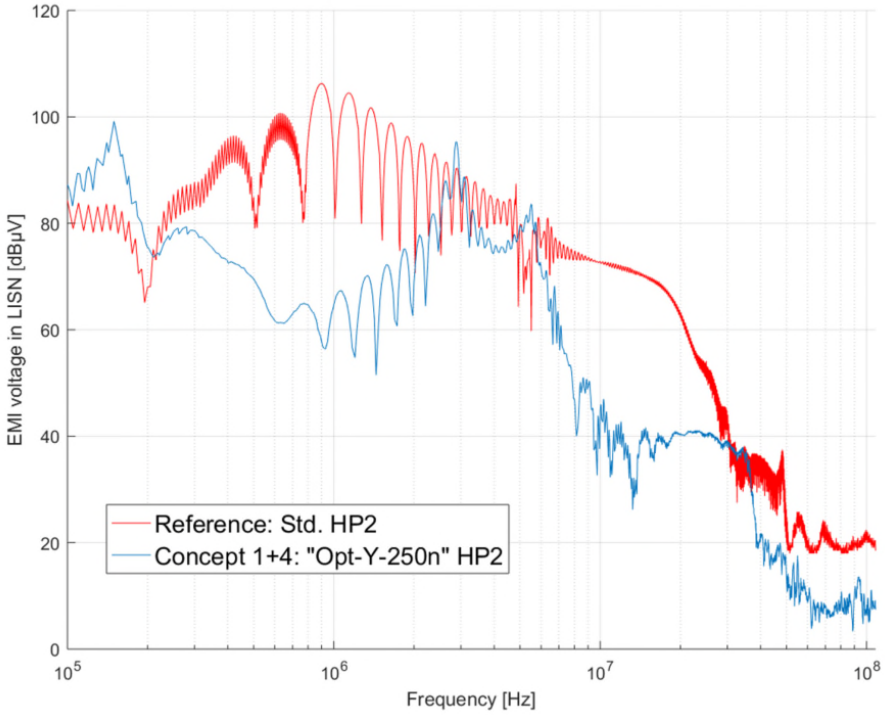


Fig. 6-22: Comparison of the conducted EMI spectrum (in average) between the standard HP2 and the variant power module "Opt_Y_250n", at V_{DC}=125V, I_{RMS_Load}=50A, f_{switch}=10kHz

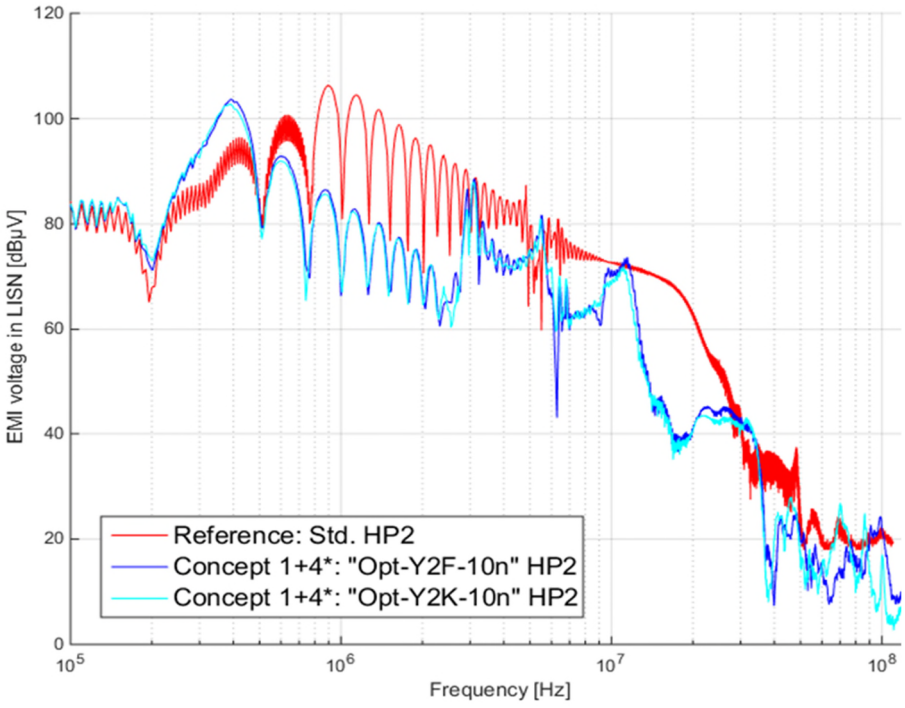


Fig. 6-23: Comparison of the conducted EMI spectrum (in average) between the standard HP2 and the variants power module "Opt_Y2F_10n" and "Opt_Y2K_10n", at V_{DC}=125V, I_{RMS_Load}=50A, f_{switch}=10kHz

6.4. Evaluation of the EMI optimization concepts

The concepts for the inherently low-interference power modules presented at beginning of this chapter are all successfully realized. The switching behavior as well as EMI performance of the prototypes are compared and analyzed in the subchapters before. From the power module manufacturer's point of view, besides the electrical performance, there are more aspects that should be taken into account regarding the evaluation of the products, especially regarding to reliability and ageing topics, if the developed power modules are designed to be used in a certain automotive application for years or even decades. Table 12 shows a summary of the advantages and disadvantages that are brought about during the realization of the EMI optimization concepts for the power module manufacturer.

First, the feasibility of prototypes should be considered since this is the first step to realize the planned concepts. In this criterion, the concept 2 and 4, by which the capacitors are installed into the power modules, are evaluated as very negatively rated. The capacitors can only be manually soldered onto the surface of the DCBs or substrates, provided that the power modules are heated over 150°C in advance. It will take more than half an hour to finish the mounting of all the needed capacitors for total 3 half-bridges in a HP2 module. The installation of the snubbers from IISB by concept 3 is different. Since the components are bare-die-shaped, they can be soldered and bonded together with the IGBTs and diodes during the chip-soldering and bonding process. The additional handling after the system-soldering process is therefore skipped.

Second, from the production's point of view, it is necessary to find out if it is feasible to produce the power modules on a large scale after the EMI optimization, especially in the existing production line. Because of the aforementioned reason by prototyping, the mounting of the capacitors into the power module can lead to extra effort for the production line. Here the mounting of the X-capacitors shall be easier than the Y-capacitors, since the soldering of the X-capacitors within the module DCB can be done during the module system-soldering process, provided that the processes and devices in the production line are adapted in advance. As for the mounting of the Y-capacitors, since several cuttings on the power module frame are necessary in order to provide sufficient space for the capacitors' connection between DC+/- and the module substrate, the large-scale production of such variants will be much harder than the standard modules. However, if the frame supplier can provide the modification of module housing in advance, then the Y-capacitor can be integrated constructively without extra expenditure. For both of the feasibility criteria for module prototyping and production, the concept 1: symmetrization of the DCB layout is evaluated as "no effect", since the changing and redesign of the layout will bring negligible effect to the manufacture.

Third, the reliability of the power module over lifetime is another important criterion. The integration of the bare-die-shaped snubber is considered to be not influential on the power module reliability, while the DCB layout changing will make the current distribution (see chapter 6.1.2) and the heat dissipation of the semiconductor chips deteriorate, thus reducing the lifetime of the power module. The HP2 module equipped with the X- and Y-capacitors is evaluated as much less reliable compared to the standard HP2, because it has higher failure

potential during the standard quality tests for the power module, such as thermal shock test (TST), mechanical shock test (MS), thermal cycling test (TC) and vibration test. Besides, the sealing of the package is reduced, and the isolation class of the power module is limited by the voltage class of the installed Y-capacitors, these are all relevant for the product specification.

Last, the additional costs of the product after the EMI optimization should be discussed. In the 4 concepts presented in this dissertation, the layout changing will hardly bring any effect to the cost. By the remaining 3 concepts, the costs of the external components must be calculated. However, compared to the power module itself, which is usually made by relatively expensive materials such as semiconductor chips, copper or AlSiC baseplate etc., the additional costs of the capacitors and snubbers turn out to be insignificant. Furthermore, in the automotive application, the additional high cost, volume and weight that are caused by the EMI filtering in HVDC system, can be effectively minimized by the measures of EMI optimization on power module level.

Table 12: Evaluation of the in this dissertation realized EMI optimization concepts by power module manufacturer's criteria

Criteria	Standard HP2	Concept 1: Symmetry	Concept 2: X-capacitor	Concept 3: Bare-die-shaped snubber	Concept 4: Y-capacitor
Feasibility in prototypes	o	o	--	o	--
Feasibility in large-scale production	o	o	-	o	--
Expected module reliability over lifetime	o	-	--	o	--
Impact on module costs	o	o	-	-	-
Expected impact on system costs	o	+	+	+	+
EMI attenuation according to CISPR-25	o	+	+	o	++
-- very negative - negative o no effect + positive ++ very positive					

7. Summary and future prospects

Power electronic components, such as the power semiconductor modules used in hybrid and electric vehicles, have high electromagnetic interference potential due to their basic mode of operation. Controlling this interference in the vehicle is an essential key to the requirements of the functional safety, and thus the sustainable market success of these components. The rising cost pressure of the competitive market leads to the demand for technical solutions that can reduce the need for expensive shielding and filtering measures. The approach of designing the semiconductor module, by which the passive electronic components (especially capacitors with low inductive connection) are located near to the interference source to reduce EMI, is therefore indispensable for achieving these goals.

As this dissertation serves as a contribution to improve the EMI performance of electrical drive systems in vehicles, the focus of the research is on the power semiconductor module for automotive application. Thereby, the power module's conducted EMI mechanisms and effects in the drive system are investigated through simulations as well as measurements. After that, the concrete EMI optimization concepts for an inherently low-interference power module are developed and realized, then evaluated by different criteria. Furthermore, a novel test procedure is introduced, by which it is possible to estimate the conducted EMI performance of power modules without parameterizing the system environment.

First of all, for a better and deeper understanding of the conducted EMI source, the switching edges respectively the high frequency pulses, which are generated during the operation of the power semiconductors, are investigated. The differences of buck-converter operation and three phase inverter operation are therefore compared. The rising as well as falling edges with different $\mathrm{dv/dt}$ caused by inconstant load currents are identified as the main reasons for the differences between the two operational modes. The influence of the diode recovery effects on the EMI performance is investigated with different load currents: Under low load current, the type of edges caused by diode reverse recovery process is more critical for the conducted EMI spectrum than the type of edges caused by starting diode free-wheeling process is; However, this situation turns out to be opposite when the load current increases. The mechanisms are interpreted as follows: Because of its inconstant load current (normally sinusoidal), the inverter operation always outspreads more emissions (in average) than the buck-converter operation in high frequency area. As a further step of the work, the influence of the diode recovery effects on the EMI performance is also investigated with different types of diodes. It has been expected that a certain EMI reduction can be achieved by replacing a snappy diode with a SiC diode by removing the reverse recovery current. However, it is confirmed in the measurements that the turn-off current of the SiC diode with extremely high $\mathrm{di/dt}$ can lead to overvoltage as well as oscillation during the commutation, which can further transform to an obvious peak at approximately 20 MHz in the EMI spectrum. Generally, the power module with SiC diodes shows higher conducted EMI (especially at approx. 20 MHz) than the standard power module because of this extra oscillation.

After the investigations of the EMI source, the discussion is stretched into the level of the drive system in the automotive application. The simulation models, which are developed and extended in this dissertation, are usable under certain boundary conditions for future power module designs with regard to the EMI prediction. The main effort during the construction of the simulation models is the determination of the parasitic elements in the drive system. The parameters not belonging to the power module, e.g. the LISN, the HV cables, the electrical motor and the grounding, etc., are usually still unknown from the perspective of the power module manufacturer in the early development phase. The use of the simulation is therefore possible only if sufficient information about the system or an agreed measurement structure is available from the vehicle OEMs' side. If this requirement is fulfilled, it has been successfully demonstrated in this dissertation that the simulation with the use of Infineon® chip models can provide valid results and predictions. This successfully laid the foundation for how the EMI factors shall be considered in the optimization of power modules.

Furthermore, based on the understanding and the conclusions from the measurement and simulation results on system level, some ideas and solutions for the inherently low-interference power module are developed and realized in Infineon®'s HybridPACK™ 2 module package for EV application. These concepts can be summarized as follows:

- Concept 1: Symmetrization and reduction of coupling capacitances / leakage inductances through optimized DCB layout
- Concept 2: Placing extremely low-impedance X-capacitors directly in the power module
- Concept 3: Placing bare-die-shaped snubbers directly in the power module
- Concept 4: Placing extremely low-impedance tied Y-capacitors directly in the power module
- Concept 4*: Placing extremely low-impedance connected Y-capacitors with voltage class of 2 kV directly in the power module

These concepts were carried out step by step. The newly designed layout is implemented in the power module package. The assembled prototypes are characterized and researched by using diverse dynamic measurements and short-circuit tests, to specifically investigate the new current distributions of the semiconductor chips due to the changed DCB layout structure, as well as the switching losses because of the insertion of the capacitors. From the EMI attenuation's point of view, the following conclusions can be made:

- The variation of filtering concepts (on module level) and capacitance size brings attenuation in different frequency bands.
- Through this knowledge one gets the freedom / possibility to design the module according to the requirement so that the conducted EMI in relevant frequency bands can be reduced;
- The integration of RC snubbers parallel to IGBT does not bring significant benefit.
- The use of the Y capacitors according to concepts 1 + 4 / 4* shows a much stronger EMI optimization effect than the other approaches do.

After that, the advantages and disadvantages that are brought about during the realization of the EMI optimization concepts for the power module manufacturer are summarized, since there are more aspects besides the electrical performance that should be taken into account regarding the evaluation of the products from the module manufacturer's point of view, especially regarding reliability and ageing topics. For instance, the integration of capacitors will possibly lead to the reduction of the module reliability, reduce the robustness of the product in

the standard thermal shock test (TST), mechanical shock test (MS), thermal cycling test (TC) and vibration test. Therefore, some future work is recommended to extend the study and find a novel solution, in which the X/Y-capacitors can be compactly integrated into the power module, without reducing its isolation, reliability and robustness.

As another aspect of contribution, a new measurement method for EMI evaluation of power modules is introduced in this work. The motivation for the research and implementation of this method, which is named “passive measurement”, was to compare and evaluate the EMI performance of power modules with an environment-independent measurement procedure. That means only the power module itself without system components is taken into account during measurement. By the primary approach, it was impossible to find the correlations between passive measurement results and conventional EMI measurement results. However, the modified and optimized passive measurement methods developed during this work make it possible. The correlation has been verified; after the network analysis, it is justifiable to say that the deviations of the resonance frequencies delivered by the different measurement methods are not drastic, yet unavoidable. The advantage of the new method is that the parameterization of the system components is no longer necessary. The expense of building a whole drive system on the test bench as required in the conventional EMI measurement, is saved. However, one has to bear the additional effort to design and manufacture the measuring adapter. Ultimately, the passive measurement method is not designed to replace the conventional measurement method, but allows an additional promising possibility (besides the conventional measuring method) to evaluate the EMI performance of the power modules. Further research can be prospected to establish this approach towards productive use in the development of future power modules.

Finally yet importantly, from the power module manufacturer’s aspect, the research results in this dissertation are irrespective of any specific implementation of a marketable product due to their scientific and technical advancement. The knowledge that has been gained by the research during this dissertation lead to a valuable acquisition of know-how which can be used for further applications and technology development.

Bibliography

References

[1] A. DOMURAT-LINDE: *Optimierung des Störemissionsverhaltens von Leistungsmodulen im UKW-Frequenzbereich*. Dissertation, TU Berlin, 2013.

[2] E. HOENE: *Methoden zur Vorhersage, Charakterisierung und Filterung elektromagnetischer Störungen von spannungsgespeisten Pulswechselrichtern*. Dissertation, TU Berlin, 2001.

[3] A. BOGLIETTI and E. CARPANETO: *Induction motor high frequency model*. Industry Applications Conference, 1999. Thirty-Fourth IAS Annual Meeting. Conference Record of the IEEE, vol. 3, 1999, pp. 1551–1558 vol.3.

[4] S. WEBER, E. HOENE, S. GUTTOWSKI, W. JOHN, and H. REICHL: *Modelling induction machines for EMC-analysis*. Power Electronics Specialists' Conference, Aachen, 2004.

[5] S. WEBER: *Effizienter Entwurf von EMV-Filtern für leistungselektronische Geräte unter Anwendung der Methode der partiellen Elemente*. Dissertation, TU Berlin, 2007.

[6] S.WEBER, E.HOENE, S.GUTTOWSKI, W.JOHN, H.REICHL: *Über magnetische Kopplung bei Entstörkondensatoren*. EMV-Messe und Kongress, Düsseldorf, 2004.

[7] M. SCHINKEL, S. WEBER, S. GUTTOWSKI, W. JOHN and H. REICHL: *Efficient HF modeling and model parameterization of induction machines for time and frequency domain simulations*. Twenty-First Annual IEEE Applied Power Electronics Conference and Exposition, APEC '06, P. 6, 2006.

[8] H. MILOUDI, A. BENDAOUD, M. MILOUDI, S. DICKMANN and S. SCHENKE: *Common Mode and Differential Mode Characteristics of AC Motor for EMC Analysis*. International Symposium on Electromagnetic Compatibility - EMC EUROPE in Wroclaw, Poland, Sep., 2016, pp. 765 - 769.

[9] G. SKIBINSKI, J. PANKAU, R. SLADKY and J. CAMPBELL: *Generation, control and regulation of EMI from AC drives*. Industry Applications Conference, Oct. 1997, vol. 2, pp. 1571 -1583.

[10] Q. LIU, W. SHEN, F. WANG, D. BOROYEVICH, V. STEFANOVIC and M. ARPILLIERE: *Experimental evaluation of IGBTs for characterizing and modeling conducted EMI emission in PWM inverters*. In Power Electronics Specialist Conference, 2003. PESC '03. 2003 IEEE 34th Annual, 2003.

[11] S. SCHULZ: *Untersuchung und Optimierung der elektromagnetischen Verträglichkeit von Umrichtern unter besonderer Berücksichtigung von Aufbautechnik und Ansteuerung der Leistungshalbleiter*. Dissertation, Otto-von-Guericke-Universität Magdeburg, 2013.

[12] F. JENNI and D. WÜST: *Steuerverfahren für selbstgeführte Stromrichter*. Vdf Hochschulverlag AG Teubner B.G. GmbH, 1995, ISBN 3-7281-2141-X.

[13] P. KLAUS: *Why diode softness matters? Understanding the switching characteristics of fast diodes and their impact on EMI and voltage stress*. In Proc. Telecommun. Energy Conf., vol. 1, Oct. 2013, pp. 162–166.

[14] X. YUAN, S. WALDER and N. OSWALD: *EMI Generation Characteristics of SiC and Si Diodes: Influence of Reverse-Recovery Characteristics*. IEEE Transactions on Power Electronics, Vol. 30, No. 3, Mar. 2015.

[15] F. LIN and D. CHEN: *Reduction of Power Supply EMI Emission by Switching Frequency Modulation*. IEEE Transactions on Power Electronics, Vol. 9, No. 1, January 1994.

[16] M. HERMWILLE: *IGBT Driver Calculation*. Application Note AN7004, SEMIKRON, 2007.

[17] J. Paramesh and A. von Jouanne: *Use of Sigma–Delta Modulation to Control EMI from Switch-Mode Power Supplies*. IEEE Transactions on Industrial Electronics, Vol. 48, No. 1, February 2001.

[18] G. ZOU, Z. ZHAO and L. YUAN: *Study on DC busbar structure considering stray inductance for the back-to-back IGBT-based converter*. Applied Power Electronics Conference and Exposition (APEC), 2013 Twenty-Eighth Annual IEEE, P. 1213-1218, 2013.

[19] N. ZHANG, S. WANG and H. ZHAO: *Develop Parasitic Inductance Model for the Planar Busbar of an IGBT H Bridge in a Power Inverter*. IEEE Transactions on Power Electronics, Vol. 30, No. 12, December 2015.

[20] S. BASU and T. M. UNDELAND: *Diode recovery characteristics considerations for optimizing EMI performance of continuous mode PFC converters*. Power Electronics and Applications, P.9, Dresden, Germany, 2005.

[21] Q. JI, X. RUAN, M. XU and F. YANG: *Effect of duty cycle on common mode conducted noise of DC-DC converters*. IEEE Energy Conversion Congress and Exposition, P. 3616 - 3621, 2009.

[22] C. PURCAREA, P. MUTSCHLER, O. MAGDUN, A. ROCKS and A. BINDER: *Time domain simulation models for inverter-cable-motor Systems in Electrical drives*. Power Electronics and Applications, EPE '09, 13th European Conference, P. 1-10, 2009.

[23] F. SHIH, D. Y. CHEN, Y. WU and Y. CHEN: *A procedure for designing EMI filters for AC line applications*. IEEE Transactions on Power Electronics, Vol. 11, P. 170-181, 1996.

[24] T. NUSSBAUMER, M. L. HELDWEIN and J. W. KOLAR: *Common mode EMC input filter design for a three-phase buck-type PWM rectifier system*. Twenty-First Annual IEEE Applied Power Electronics Conference and Exposition, APEC '06, P. 7, 2006.

[25] S. OGASAWARA and H. AKAGI: *Modeling and damping of high-frequency leakage currents in PWM inverter-fed AC motor drive systems*. IEEE Transactions on Industry Applications, Vol. 32, P. 1105-1114, 1996.

[26] W. P. SIEBERT: *Cooling Structure for EMC Shielded High Frequency Electronics*. IEEE Transactions on Components and Packaging Technologies, Vol. 29, No. 1, March 2006.

[27] J. LU and F. DAWSON: *EMC Computer Modeling Techniques for CPU Heat Sink Simulation*. IEEE Transactions on Magnetics, Vol. 42, No. 10, October 2006.

[28] J. LU, B. ZHU, and D. THIEL: *Full Wave Solution for Intel CPU with a Heat Sink for EMC Investigations*. IEEE Transactions on Magnetics, Vol. 46, No. 8, August 2010.

[29] S. MANIVANNAN, R. ARUMUGAM, S. P. DEVI, S. PARAMASIVAM, P. SALIL and B. SUBBARAO: *Optimization of heatsink EMI using Design of Experiments with numerical computational investigation and experimental validation*. Electromagnetic Compatibility (EMC), IEEE International Symposium, P. 295-300, 2010.

[30] X. GONG and J. A. FERREIRA: *Reduction of conducted EMI for SiC JFET inverters by separating heat sinks*. IEEE 7th International Power Electronics and Motion Control Conference - ECCE Asia, P. 1070 - 1077, June 2012.

[31] X. GONG and J. A. FERREIRA: Extracting the parameters of a common mode EMI equivalent circuit model for a drive inverter. The 2010 International Power Electronics Conference, P. 892 - 899, 2010.

[32] J. Z. CHEN, L. YANG, D. BOROYEVICH and W. G. ODENDAAL: *Modeling and measurements of parasitic parameters for integrated power electronics modules*. Applied Power Electronics Conference and Exposition, APEC '04, Vol. 1, P. 522 - 525, 2004.

[33] A. NEJADPAK and O. A. MOHAMMED: *Physics-Based Modeling of Power Converters from Finite Element Electromagnetic Field Computations*. IEEE Transactions on Magnetics, Vol. 49, No. 1, January 2013.

[34] C. HOER and C. LOVE: *Exact Inductance Equations for Rectangular Conductors with Applications to More Complicated Geometries*. National Bureau of Standards-C, Engineering and Instrumentation, Vol. 69C, No.2, 1965.

[35] A. E. RUEHLI: *Inductance Calculations in a Complex Integrated Circuit Environment*. IBM Journal Research and Development, 1972.

[36] R. BAYERER: *Power Circuits for Clean Switching and Low Losses*. ECPE Tutorial, Ch. 5, Düsseldorf, Germany, 2016.

[37] S. KOCHETOV and T. SMAZINKA: *Methodologie und Prüfverfahren zur EMV Qualifizierung von Leistungsmodulen*. Internationale Fachmesse und Kongress für Elektromagnetische Verträglichkeit, Düsseldorf, Germany, February 2016.

[38] INFINEON TECHNOLOGIES AG: *BMBF-Verbundprojekt EM4EM: Elektromagnetische Zuverlässigkeit und elektronische Systeme für eMobility-Anwendungen: Teilvorhaben: EMZ-spezifizierte leistungs- /nano- /mikroelektronische Bauelemente und Komponenten für eMobility-Anwendungen : Berichtszeitraum: 1. Oktober 2011-31. März 2015*. TIB/BMBF-Bibliothek, Neubiberg, 2015.

[39] INFINEON TECHNOLOGIES AG: *AN2011-05 Industrial IGBT Modules Explanation of Technical Information*. Application Note AN 2011-05 V1.2 November 2015, Warstein, 2015.

[40] P. HILLENBRAND, S. TENBOHLEN, C. KELLER and K. SPANOS: *Understanding conducted emissions from an automotive inverter using a common-mode model*. 2015 IEEE International Symposium on Electromagnetic Compatibility (EMC), P. 685-690, 2015.

[41] J. HANSEN: *EMC Simulation of 48V Systems*. 1st International Conference Electromagnetic Compatibility of Future Cars, Berlin, Germany, April 2015.

[42] S. KIM and D. P. NEIKIRK: *Compact equivalent circuit model for the skin effect*. Microwave Symposium Digest, Vol. 3, P. 1815-1818, 1996.

[43] Y. WEENS, N. IDIR, R. BAUSIÈRE, and J. J. FRANCHAUD: *Modeling and Simulation of Unshielded and Shielded Energy Cables in Frequency and Time Domains*. IEEE Transactions on Magnetics, Vol. 42, No. 7, July 2006.

[44] C. MARLIER, A. VIDET and N. IDIR: *NIF-Based Frequency-Domain Modeling Method of Three-Wire Shielded Energy Cables for EMC Simulation*. IEEE Transactions on Electromagnetic Compatibility, Vol. 57, P. 145-155, 2015.

[45] J. R. MOSER: *Peripheral Cable-Shield Termination: The System EMC Kernel*. IEEE Transactions on Electromagnetic Compatibility, Vol. 28, No. 1, 1986.

[46] B. K. SEN and R. L. WHEELER: *Skin effects models for transmission line structures using generic SPICE circuit simulators*. Electrical Performance of Electronic Packaging, IEEE 7th Topical Meeting, P. 128-131, 1998.

[47] C. YEN, Z. FAZARINC and R. L. WHEELER: *Time-domain skin-effect model for transient analysis of lossy transmission lines*. Proceedings of the IEEE, Vol. 70, No. 7, 1982.

[48] X. ZENG, X. YANG and Z. WANG: *Analysis of electromagnetic coupling in hybrid integrated power electronic module*. Power Electronics Specialists Conference, PESC 04, 2004 IEEE 35th Annual, Vol. 6, P. 4509-4515, 2004.

[49] J. BAUCH, S. SCHULZ and A. LINDEMANN: *Influence of Parasitic Capacitive Currents on Conducted Emissions of Power Converters*. 9th International Multi-Conference on Systems, Signals and Devices (SSD), 2012.

[50] F. KLOTZ: *Leitungsgebundene elektromagnetische Stoeremissionen von Leistungshalbleitertopologien*. Ph.D.thesis, Technische Universitaet Ilmenau, 1997.

[51] A. NAGEL: *Leitungsgebundene Störungen in der Leistungselektronik: Entstehung, Ausbreitung und Filterung.* Dissertation, Rheinisch-Westfaelische Hochschule Aachen, 2001.

[52] A. MUSING, M. L. HELDWEIN, T. FRIEDLI and J. W. KOLAR: *Steps towards Prediction of Conducted Emission Levels of an RB-IGBT Indirect Matrix Converter*. Power Conversion Conference - Nagoya, P. 1181-1188, 2007.

[53] M. L. HELDWEIN: *EMC Filtering of Three-Phase PWM Converters.* Ph.D.thesis, ETH ZÜRICH, 2008.

[54] K. KAM, D. POMMERENKE, F. CENTOLA, C. LAM and R. STEINFELD: *EMC Guideline for Synchronous Buck Converter Design*. IEEE International Symposium on Electromagnetic Compatibility, P. 47-52, 2009.

[55] J. FUENTES: *Predicting and Comparing Conducted EMI of Power Modules by Using Double-Pulse Measurements Results and Simulation*. Masterarbeit, Technische Universität Dortmund, Aug. 2015.

[56] S. WANG and F. C. LEE: *Common-Mode Noise Reduction for Power Factor Correction Circuit with Parasitic Capacitance Cancellation*. IEEE Transactions on Electromagnetic Compatibility, Vol. 49, No. 3, August 2007.

[57] S. WANG and F. C. LEE: *Investigation of the Transformation Between Differential-Mode and Common-Mode Noises in an EMI Filter Due to Unbalance*. IEEE Transactions on Electromagnetic Compatibility, Vol. 52, No. 3, August 2010.

[58] G. GRANDI, D. CASADEI and U. REGGIANI: *Common- and differential-mode HF current components in AC motors supplied by voltage source inverters*. IEEE Transactions on Power Electronics, Vol. 19, No. 1, January 2004.

[59] W. FAN, A. LU, L. L. WAI, and B. K. LOK: *Mixed-mode S-parameter characterization of differential structures*. Electronics Packaging Technology, 2003 5th Conference (EPTC 2003), P. 533- 537, 2003.

[60] C. CHRISTOPOULOS: *Principles and Techniques of Electromagnetic Compatibility, Second Edition*. Taylor & Francis, 2007.

[61] *Code of Federal Regulations*. Title 47 (47CFR), Part 15.

[62] VDE 0839 Teil 6-1 2007-10 DIN EN 61000-6-1: *Elektromagnetische Verträglichkeit (EMV) - Teil 6-1: Fachgrundnormen Störfestigkeit für Wohnbereich, Geschäfts- und Gewerbebereiche sowie Kleinbetriebe* (IEC 61000-6-1: 2005) Deutsche Fassung EN 61000-6-1: 2007. Norm, 2007.

[63] VDE 0839 Teil 6-2 2006-03 DIN EN 61000-6-2: *Elektromagnetische Verträglichkeit (EMV) - Teil 6-2: Fachgrundnormen Störfestigkeit für Industriebereich* (IEC 61000-6-2:) Deutsche Fassung EN 61000-6-2: 2005. Norm, 2006.

[64] VDE 0839 Teil 6-3 2011-09 DIN EN 61000-6-3: *Elektromagnetische Verträglichkeit (EMV) - Teil 6-3: Fachgrundnormen Störaussendung für Wohnbereich, Geschäfts- und Gewerbebereiche sowie Kleinbetriebe* (IEC 61000-6-3: 2006 + A1: 2010) Deutsche Fassung EN 61000-6-3: 2007 + A1: 2011. Norm, 2011.

[65] VDE 0839 Teil 6-4 2011-09 DIN EN 61000-6-4: *Elektromagnetische Verträglichkeit (EMV) - Teil 6-4: Fachgrundnormen Störaussendung für Industriebereich* (IEC 61000-6-4: 2006 + A1: 2010) Deutsche Fassung EN 61000-6-4: 2007 + A1: 2011. Norm, 2011.

[66] VDE 0160-103 2019-04 DIN EN 61800-3: *Drehzahlveränderbare elektrische Antriebe – Teil 3: EMV-Anforderungen einschließlich spezieller Prüfverfahren* (IEC 61800-3:2017) Deutsche Fassung EN 61800-3: 2018. Norm, 2018.

[67] CISPR 25: *Radio disturbance characteristics for the protection of receivers used on board vehicles, boats, and on devices - Limits and Methods of Measurement*. 2016.

[68] D. E. BOCKELMAN and W. R. EISENSTADT: *Combined differential and common-mode scattering parameters: theory and simulation*. IEEE Transactions on Microwave Theory and Techniques, Vol. 43, No. 7, July 1995.

[69] N. OKA, T. KUMAMOTO, K. MISU and S. NITTA: *Differential mode Noise on the PCB's Signal Traces Converted from External Common mode Noise*. 2009 IEEE International Symposium on Electromagnetic Compatibility, P. 166-170, 2009.

[70] M. KAMIKURA, Y. MURATA and A. NISHIZAWA: *Investigation on the mode conversion between common-mode and differential-mode noises in EMI filters for power electronics circuits*. Proc. of the 2013 International Symposium on Electromagnetic Compatibility (EMC Europe 2013), Brugge, Belgium, September, 2013.

[71] S. SCHEFLER, M. PUFF, M. KOINI and S. WEBER: *Modelling an anti-ferroelectric ceramic capacitor for time-and frequency-domain simulations of power systems.* PCIM, Nuremberg, Germany, 2016.

[72] D. SCHRÖDER: *Leistungselektronische Bauelemente (Bd. 3)*. Springer Verlag Berlin Heidelberg, 2006.

[73] R. BAYERER and D. DOMES: *Power circuit design for clean switching*. CIPS 2010, Nürnberg, 2010.

[74] A. BRODT: *Aussagen zur geleiteten Störemission in Wechselrichtern auf Basis des IGBT Schaltverhaltens*. Masterarbeit, Universität Duisburg-Essen, Dec. 2014.

[75] *DIRECTIVE 2014/30/EU OF THE EUROPEAN PARLIAMENT AND OF THE COUNCIL of 26 February 2014 on the harmonisation of the laws of the Member States relating to electromagnetic compatibility (recast)*. Official Journal of the European Union, p. 96/84, 2014.

[76] C. R. PAUL: *Introduction to Electromagnetic Compatibility*. Wiley Series in Microwave & Optical Engineering, Feb 2006.

[77] J. LUTZ: *Halbleiter-Leistungsbauelemente*. 2. Auflage, Springer Verlag.

[78] Y. H. LEE and A. NASIRI: *Analysis and modeling of conductive EMI noise of power electronics converters in electric and hybrid electric vehicles*. Twenty-Third Annual IEEE Applied Power Electronics Conference and Exposition, p. 1952-1957, 2008.

[79] S. QU and D. CHEN: *Mixed-mode EMI noise and its implications to filter design in offline switching power supplies*. IEEE Transactions on Power Electronics, vol. 17, no. 4, pp. 502-507, Jul 2002.

[80] M. SCHINKEL: *Entwurf und Simulation aktiver EMV-Filter für dreiphasige drehzahlveränderbare Antriebe*. Dissertation, TU Berlin, 2009.

[81] J. WALKER: *Handbook of RF and Microwave Power Amplifiers*. Cambridge University Press, 2012.

[82] K. SPANOS, C. KELLER, M. BÖTTCHER and E. SCHULTE BOCHOLT: *Abschlussbericht zum Verbundprojekt Inhärent Störungsarme Leistungselektronik - 'InSeL' : Projektlaufzeit: 1. Januar 2014 - 31*. Dezember 2016. V1-0. TIB/BMBF-Bibliothek, Robert Bosch GmbH, Stuttgart, 2017.

[83] S. KOCHETOV: *Schlussbericht der Bayerischen Motoren Werke Aktiengesellschaft über das Förderprojekt: InSeL - Inhärent Störungsarme Leistungselektronik : Laufzeit: 01.01.2014-31.12.2016*. TIB/BMBF-Bibliothek, Bayerische Motoren Werke Aktiengesellschaft, München, 2017.

Online Sources

[84] INFINEON TECHNOLOGIES AG: *HybridPACK™ 2: Power Module for Hybrid- and Electric Vehicles*. Product brief, Neubiberg, 2012. [Online]. Available: https://www.infineon.com/dgdl/Infineon-HybridPACK2_Power_Modules-PB-v01_00-EN.pdf (visited on Apr. 15, 2014).

[85] INFINEON TECHNOLOGIES AG: Technical Information FS800R07A2E3_B31 *HybridPACK™ 2 Module, V3.1.* Data sheet, Neubiberg, 2014. [Online]. Available: https://www.infineon.com/cms/de/product/power/igbt/automotive-qualified-igbts/automotive-igbt-modules/ (visited on Jul. 10, 2014).

[86] ROGERS CORPORATION: *Curamik® CERAMIC SUBSTRATES DBC technology DESIGN RULES Version 12/2014*. Eschenbach, 2014. [Online]. Available: https://www.rogerscorp.com/documents/3061/curamik/Design-Rules---DBC-Technology.pdf (visited on Oct. 23, 2016).

[87] TDK ELECTRONICS AG: *CeraLink® Capacitors for fast-switching semiconductors – Low profile (LP) series (Ordering code: B58031*), V6.1*. Data sheet, 2019. [Online]. Available: https://www.tdk-electronics.tdk.com/inf/20/10/ds/B58031_LP.pdf (visited on Jun. 03, 2019).

[88] TDK ELECTRONICS AG: *CeraLink® Capacitors for fast-switching semiconductors – Flex Assembly (FA) series (Ordering code: B58035U*), V6.0*. Data sheet, 2019. [Online]. Available: https://www.tdk-electronics.tdk.com/inf/20/10/ds/B58035_FA.pdf (visited on Jun. 03, 2019).

[89] FRAUNHOFER IISB: *Monolithic RC-snubbers and capacitors up to 600V*. Data sheet, 2014. [Online]. Available: https://www.iisb.fraunhofer.de/content/dam/iisb2014/en/Documents/Research-Areas/Devices/Downloads/FraunhoferIISB_ProductSheet_DEV_Monolithic-RC-Snubbers-and-Capacitors_WWW.pdf (visited on Jul. 08, 2015).

Publications

The work in this dissertation has resulted in the following publications:

[90] Y. LIU, S. CORDES, T. GEINZER, J. THIELE, M. THOBEN and A. LINDEMANN: *Comparison of EMI behavior in inverter and buck-converter operation of power modules by considering the diode reverse recovery effects*. CIPS 2016, 9th International Conference on Integrated Power Electronics Systems, Nürnberg, 2016.

[91] Y. LIU, S. KOCHETOV, T. SMAZINKA and A. LINDEMANN: *Characterizing the Conducted EMI Performance of a Power Module through Passive Measurement*. PCIM Europe 2017, International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, Nürnberg, 2017.

[92] Y. LIU, T. GEINZER, S. CORDES and J. THIELE: *Inhärent Störungsarme Leistungselektronik - InSeL : Teilvorhaben: Infineon Technologies AG : EMV-gerechtes Design von Leistungselektronikmodulen für Automotive-Anwendungen : Schlussbericht InSeL : Berichtszeitraum: 01.01.2014 bis 31.12.2016*. TIB/BMBF-Bibliothek, Infineon Technologies AG, München, 2017.

The contents of the above publications have been used directly or indirectly in this dissertation.

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