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Chapter 3 will introduce the interactions of the mechanical stress, the temperature and the electric field. The effects connecting these state variables are explained in detail and it will be shown which effects can be neglected and which ones need closer investigations.
In Chapter 4 the thermal capabilities under massive thermal overload, caused by a short circuit pulse, are discussed. The setup, which is used to stress the chips until failure, is presented. Failed devices are analyzed extensively by in depth physical failure inspection methods. Root cause analysis is done by means of Finite Element Analysis (FEA) and in depth physical failure analysis, finally enabling to provide suggestions for improvements in this particular failure mode.
Chapter 5 will elaborate on resonance phenomena in GaN. Since GaN is piezoelectric it can act as an actuator to resonate the whole chip assembly. This phenomenon is measured in two steps and subsequently investigated by FEA. The Finite Element (FE) simulation results are validated against the measurements to ensure the correctness of the FE model. From these simulations conclusions regarding the reliability of the two most failure prone layers, namely the GaN stack and the die attach layer, are drawn. Additionally extreme cases are discussed giving an outlook on this issue in advanced package assemblies.

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Gallium Nitride (GaN) specific mechanical phenomena and their influence on reliability in power HEMT operation

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Contents

Abstract

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Zusammenfassung

In den letzten Jahren ist Gallium Nitride (GaN) auf dem Markt für Leistungsbauelemente in größerem Maßstab angekommen, wodurch die Notwendigkeit eines tieferen Verständnisses der grundlegenden Interaktionen im Chip notwendig geworden ist. Umfangreiche Forschung wurde auf dem Gebiet der elektrischen Effekte durchgeführt, da dort die wichtigsten Unterschiede gegenüber Silicon (Si) liegen. Im Gegensatz zur generellen Forschungsrichtung fokussiert sich diese Arbeit auf neue mechanische und thermo-mechanische Phänomene, die bisher in Si Bauteilen nicht vorhanden waren.

In Kapitel 3 wird die Wechselwirkung von mechanischer Spannung, Temperatur und elektrischem Feld besprochen. Die physikalischen Effekte, die diese Zustandsgrößen verbinden, werden im Detail erklärt und es wird gezeigt, welche Effekte aufgrund ihrer Größe sicher vernachlässigt werden können und welche einer näheren Untersuchung bedürfen.

In Kapitel 4 werden die thermischen Fähigkeiten bei massiver thermischer Überlastung, die durch einen Kurschluss verursacht wird, diskutiert. Der Testaufbau, auf dem die Chips bis zum Ausfall gestresst werden, wird vorgestellt. Anschließend werden die ausgefallenen Bauelemente analysiert und die Grundursache mit Hilfe von der Finite Element Analysis (FEA) und einer umfassenden, detaillierten physikalischen Fehleranalyse erklärt. Zusätzliche Vorschläge für Verbesserungen in diesem speziellen Versagensmodus werden am Ende gegeben.

Kapitel 5 gibt Einblicke in die Resonanzphänomene bei GaN. Da GaN piezoelektrisch ist kann es als Aktuator fungieren, um den gesamte Chip in Resonanz zu bringen. Dieses Phänomen ist vermessen worden und wird anschließend durch FEA simuliert. Die Simulation wird dann gegen die Messung validiert, um die Richtigkeit der Simulation sicherzustellen. Aus diesen Simulationen werden Schlussfolgerungen bezüglich der Zuverlässigkeit der beiden am meisten gefährdeten Schichten, der GaN Schicht und Chip Verbindungsschicht, gezogen. Zusätzlich werden am Ende Extremfälle diskutiert, die einen Ausblick auf kommende Chipgehäuse geben sollen.

Nekrolog

In the memory of my beloved mother,
who died while writing this thesis.

Our time together was way too short.

Хотели лучше, но получилось как всегда.

(We wanted to do better, but it worked out as usual.)
russian proverb

Chapter 1

Motivation

Gallium Nitride (GaN) is a new material advertised for power High Electron Mobility Transistors (HEMTs) since about 12 years. It was extensively studied with respect to device functionality and instabilities, whereas this thesis concentrates on aspects not covered so far, and which are typical for power (high voltage, high current and high temperature) applications, and where we may expect new mechanisms and failure modes. For a start some aspects of the GaN material and the power applications will be highlighted.

1.1 Gallium Nitride

Gallium nitride is a III/V semiconductor with a direct band gap that recently entered the power semiconductor market in big quantities. It is a brittle and transparent material, which can have two different crystal structures. To be more precise GaN can appear in the so called Wurtzite or Zincblende structure [LRS01], whereas the first one is used in semiconductors and shown in Figure 1.1.

Table 1.1: Comparison of basic properties of Silicon, Gallium nitride and Silicon carbide [Bol18].

	Si	**GaN**	**SiC**
Band gap (eV)	1.1	3.4	3.2
Breakdown field (V/cm)	3×10^5	4×10^6	4×10^6
Thermal conductivity (W/(m K))	150	130	370
Coefficient of thermal expansion (10^{-6}/K)	3.6	3.2	2.4

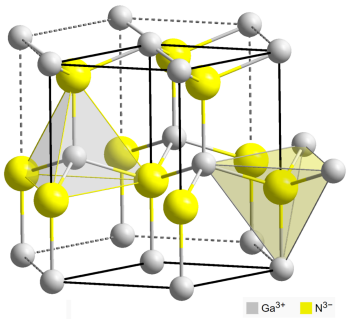


Figure 1.1: GaN Wurtzite structure [08]

Due to its crystal structure $P6_3mc$, GaN has pyroelectric properties, which means it reacts with charge separation to temperature changes, and piezoelectric properties [KPG08], which means it reacts with an electric field to deformation. This crystal structure is asymmetric with respect to its centers of positive and negative charge, which also results in a spontaneous polarization. This spontaneous polarization combined with a polarization from tensile or compressive stress can be used to form a two-dimensional electron gas (2DEG), which is necessary to construct a HEMT.

1.1.1 Device

Due to nature of the 2DEG forming on the border between GaN and Aluminium Gallium Nitride (AlGaN) nearly all devices are build laterally. As will be described in more detail later, the lateral devices comprised of source and drain fingers interlinking forming a sequence of lateral single cells (see Figure 4.6) The gate control is situated lower in the stack and funneled under the source to the gate fingers.

In principle GaN HEMTs can be divided in two different categories by the way they are operated. Depletion mode HEMTs, also called normally on HEMTs, can just be switched off if the 2DEG is depleted by applying a negative voltage to the gate. This kind is not preferable, since in absence of a gate voltage the transistor is on, which can lead to more circuit effort, so that during power up or failure situations no dangerous situation is triggered. The second type are enhancement mode HEMTs, or short eHEMTs. This type of chips can be manufactured by featuring a technology that normally depletes the 2DEG under the gate by a p-GaN making them normally off.

1.1.2 Production

The commercial production of GaN HEMTs is nearly exclusive in a GaN on Silicon (Si) technology, because of two main reasons. First, that GaN cannot be produced monocrystalline in big diameters like Si. Second, with a GaN on Si technology it is possible to use the vast variety of machines and methods already present for Si wafers.

Unfortunately GaN and Si feature different lattice constants, 3.19 Å for GaN compared to 3.84 Å in <111> Si. This difference makes it necessary to grow adaption layers on the Si wafer in order to grow a defect free GaN layer on top, which acts as substrate for the further device production. The two most common approaches for the adaption layer are a graded approach and a superlattice approach. In the graded approach several layers of AlGaN with ever more decreasing aluminum percentage are stacked on top of each other. A high number (e.g. 100) of GaN and Aluminium Nitride (AlN) layers are stacked alternately above each other, when applying the superlattice approach. On top of these adaption layers a relatively defect free monocrystalline GaN can be grown acting as substrate for the subsequent device production with classical methods and tools used in Si devices. The completely manufactured chip is than mounted into an assembly.

1.2 Power electronics

Even tough a GaN transistor utilizes a completely different principle than Si transistors, it features the same nomenclature, with gate, drain and source. The main differences to a Metal-Oxide Semiconductor Field Effect Transistor (MOSFET) are the following: Due to the conduction layer (2DEG) existing in a quantum well of a GaN HEMT, the R_{on} is lower than in MOSFET devices [Eve+10]. Featuring an intrinsically higher breakdown field of the base material, chips can be built smaller to achieve same breakdown voltages.

As described above, there are two types of GaN HEMTs. Normally off GaN HEMTs are the natural choice to replace MOSFETs.

A further fundamental advantage of GaN HEMTs over common MOSFETs are significantly smaller intrinsic capacities (C_{GD}, C_{GS}) due to the structure as a lateral device. The area of capacitor between gate and drain (C_{GD}) is just the small gate side facing the drain resulting in very low capacity. The capacity between gate and source C_{GS} results from the other small gate side facing the source and the dielectric between the gate and the source field plate (compare Figure 4.7).

Drawbacks in GaN devices arise from the fact that they are lateral devices with a complicated material stack which feature a challenging R_{th} behavior. A major further challenge in manufacturing these devices is their dynamic on resistance $R_{DS(on)}$. This dynamic effect results from captured charges in various regions and is still not fully understood.

Another feature worthwhile mentioning is that GaN HEMTs feature a behavior acting in the same manner as an intrinsic body diode, which is necessary in certain topologies as for example buck converters. With a negative voltage between gate and source, turning off the device leads to a positive bias on the gate versus the drain potential. This makes the device conduct in reverse direction, acting similarly to a body diode in Si devices.

Theoretically a GaN device is a symmetric device, just by the realization of a cell, the voltage limits in the forward and reveres direction are different, making it asymmetric.

1.3 Power conversion

GaN HEMTs are nowadays widely used to build converters. One prime example for GaN usage are power factor correction stages. Power factor correction stages are an essential part in every modern off-grid electronic device, which should feature several main characteristics among others. The power correction stage should be highly efficient in terms of energy conversion, should feature a small volume and be cheap to manufacture.

In a first order approximation one can estimate the implications on the passive elements by increasing the switching frequency by a factor m. This means to get the same inductive load X_L

$$X_L = \omega L = 2\pi f L \tag{1.1}$$

the inductance L needs to be scaled by the factor $\frac{1}{m}$. For ease of calculation a toroidal inductor is considered. Its inductance L can be calculated by

$$L \approx N^2 \frac{\mu_0 \mu_r A_{ind}}{2\pi r_{ind}}, \tag{1.2}$$

where A_{ind} depicts the cross section of the core and r_{ind} the radius of the circular ring. This results in a $\frac{1}{m}$ scaling of L with the cross-section of the magnetic core.

The time between two output peaks in a harmonic signal is also scaled by the factor $\frac{1}{m}$. This implies that the smoothing capacitor can also be scaled, since in $\frac{1}{m}$ of the time, just $\frac{1}{m}$ of the electric energy W_{el} is needed. Given a plate capacitor featuring

$$W_{el} = \frac{1}{2}\epsilon_0\epsilon_r E^2 A_{cap} d_{cap}, \tag{1.3}$$

with a plate area A_{cap} and the distance between the the plates d_{cap}, the area A_{cap} can be scaled by $\frac{1}{m}$.

Since the biggest cost factor of switched mode power supplies is the passives with up to 30 % [BK13], it maybe even from a purely economical point of view be advantageous to use GaN HEMT technology, if the savings are not eaten up by higher GaN HEMT prices. It has to be mentioned that this the cost reduction does not even take the significant size and weight reduction, due to smaller passives into account.

The effects of the switching frequency on the overall efficiency can be understood as follows. Due to smaller parasitics in smaller capacitors, already discussed above, it is possible to realize steeper $\frac{dV}{dt}$ slopes and therefore higher frequencies. These steeper slopes reduce the losses per switching event, in contrast to increasing numbers of switching events in a given time span. Hence, the increase in switching losses is counteracted by the GaN technology.

As discussed before, with higher frequencies the passive components can be shrunk. Since losses in passive components are primarily proportional to the volume, e.g. magnetic flux per volume or electric field per volume, the losses in passives decrease. This trend of course does not hold true for any frequency increase. At some point losses scaling with the frequency will start playing a more significant role. This gives an optimal frequency in terms of efficiency.

Further gains in terms of efficiency can be realized by using a soft switching instead of a hard switching topology. Such a switching principle additionally reduces the switching losses by turning the device on and off at (approximately) zero voltage or current, by using an LC resonant circuit.

Typical switching topologies used with GaN are the LLC topology and totem pole for example [Zoj18].

A bridgeless totem pole Power Factor Correction (PFC) is an evolution from a bridge rectifier with a boost converter as can be seen in Figure 1.2. The basic drawback of the bridge rectifier is the forward voltage of the diodes accounting for a big portion of the

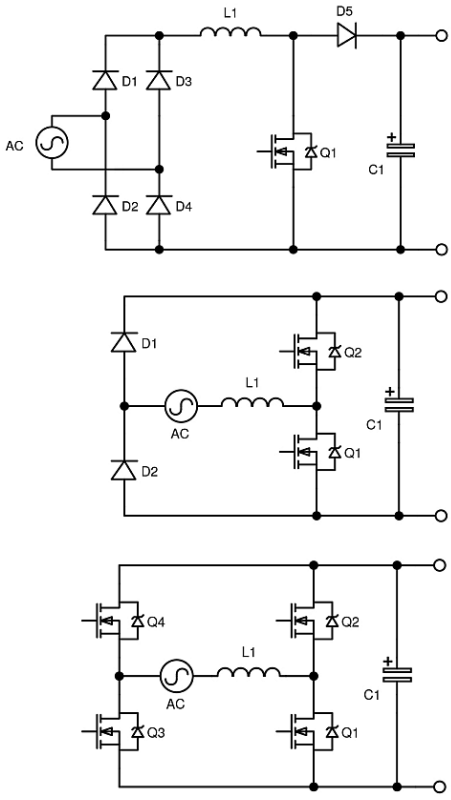


Figure 1.2: Schematics of an ordinary bridge rectifier with a boost converter evolving into a bridgeless totem pole PFC [Li20].

losses. To mitigate those losses the diodes can be switched for transistors in combination with a suitable controller.

If the transistors are designed as MOSFETs a problem arises, when the body diodes are conducting and in the next phase of the switching cycle a reverse recovery appears. These reverse recovery losses limit the usage of this switching topology at higher power levels where GaN is used. Using GaN HEMTs these losses can be completely omitted, significantly increasing the efficiency of bridgeless totem pole PFC

This combination of advantages of course come with the price of a new semiconductor material and transistor principle, which posts new opportunities and challenges in terms of reliability.

Chapter 2

Reliability engineering

Reliability is an engineering field investigating the life expectancy of a product and its function over time. In contrast to reliability, focusing on nominal use cases, robustness investigates the system behavior in off nominal regimes. Both areas must be explored for new materials to asses their strengths and weaknesses and to build robust and reliable products.

The field of reliability in terms of semiconductor can be narrowed down to the failure mechanisms of semiconductor devices, which can be categorized following [KŤ20] as follows:

- material interaction induced failure mechanisms,
  (e.g. ohmic contact degradation, surface-state effects)
- stress induced failure mechanisms,
  (e.g. electromigration, hot electron trapping)
- mechanically induced failure mechanisms
  (e.g. die fracture, solder cracks)
- environmentally induced failure failure mechanisms
  (e.g. humidity effects)

While all these failure mechanism exist, this work will focus on the high power dissipation (short circuit) and the piezoelectric effects on structural integrity of a packaged power device.

In general, the failure rate of a device can be visualized by a bathtub curve as in Figure 2.1.

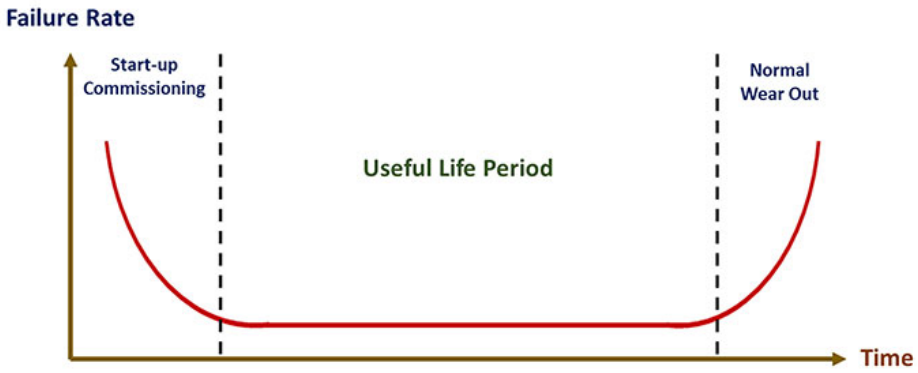


Figure 2.1: A bathtube curve describes the typical failure rate over time [Liv18].

As can be seen in Figure 2.1, in the beginning the failure rate is increased, this effect is called infant mortality. This effect is normally mitigated by careful screening or a burn in phase were early failures can be detected. After the infant mortality period, a plateau phase with a constant failure rate is reached, marking the normal lifespan. At the end of life the wear out phase follows where the failure rate increases again.

Since in Gallium Nitride (GaN) High Electron Mobility Transistors (HEMTs) the underlying principle of the transistor is changed, much attention is given to the investigation in terms of its electrical performance. The combined changes of principle and base material open a very wide field of new semiconductor phenomena.

2.1 Electrical failure modes

In commonly used Silicon (Si) devices a long research history has helped in identifying the main root causes of failures during lifetime . This deep understanding of the underlying mechanisms enabled to define a small number of tests (see Table 2.1) in order to ensure robust and reliable devices.

Since GaN, in the power device market, does not have such a long history comparable standardized tests are not available. Thus, a lot of research is still open and needs to be done. The main areas of research without the claim of being complete are summarized as below.

The main areas of today's research focus on breakdown paths and trapping sites, which are summarized below. As can be seen in Figure 2.2 (a) there are several breakdown paths.

Table 2.1: Standardized test for Si devices [KŤ20]

Abbr.	Test/Standard	Conditions	Duration	Sample size
TC	temperature cycling JESD22 A104	T = -55/150°C	1 000 times	3 lots × 77 pcs
HTRB	high temp. reverse bias JESD22 A108	V = 600 V, T = 150°C	1 000 h	3 lots × 77 pcs
HTS	high temp. storage life JESD22 A103	T = 150°C	1 000 h	3 lots × 77 pcs
HTGS(+)	pos. high temp. gate stress JESD22 A108	I = 50 mA	1 000 h	3 lots × 77 pcs
HTGS(-)	neg. high temp. gate stress JESD22 A108	V = -10 V	1 000 h	3 lots × 77 pcs
H3TRB	temp. and humidity bias JESD22 A101	V = -10 V, humidity = 85 %, T = 150°C	1 000 h	3 lots × 77 pcs
IOL	intermittent operating life test JESD22 A105	ΔT = 100°C	15 000 times	3 lots × 77 pcs
ESD	ESD-HBM and CDM JS-001 and JS-002		1 000 h	1 lot × 3 pcs

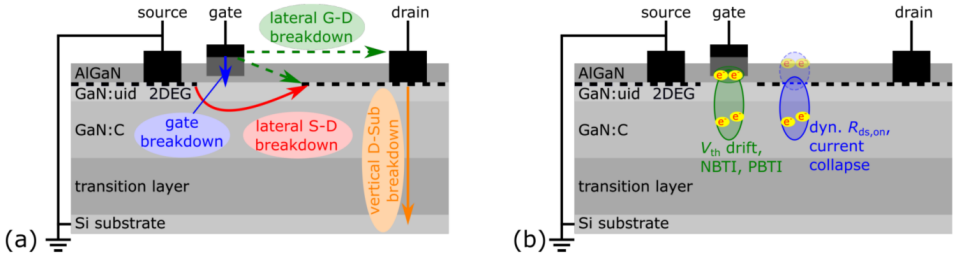


Figure 2.2: Possible break through paths of a GaN HEMT can be seen in figure (a), whereas (b) shows typical trapping sites and their effects [KŤ20].

The first one is a gate breakdown, where a conduction path is opened by an avalanche breakdown mechanism [Wu+15]. Another breakdown path is the lateral breakdown between gate and drain destroying the device [Zan+13]. The so called pinch through breakdown happens between source an drain [Zag+19]. Leakage can also occur through the buffer layer, marking the last important breakdown path [Men+15].

Additionally to breakdown paths, charge trapping effects influence the performance of GaN devices heavily. Due to charge trapping on the gate the threshold voltage V_{th} can shift significantly making it hard to control in appliances over time. As well as Silicon Carbide (SiC) Metal-Oxide Semiconductor Field Effect Transistor (MOSFET)

devices also GaN HEMTs can suffer from Negative Bias Temperature Instability (NBTI) [Ťap+13] and Positive Bias Temperature Instability (PBTI) [Ost+18]. With NBTI positive charges (holes) accumulate at the gate, shifting the threshold voltage V_{th} to lower values. Vice versa, with PBTI electrons accumulate at the gate shifting the threshold voltage V_{th} to higher values.

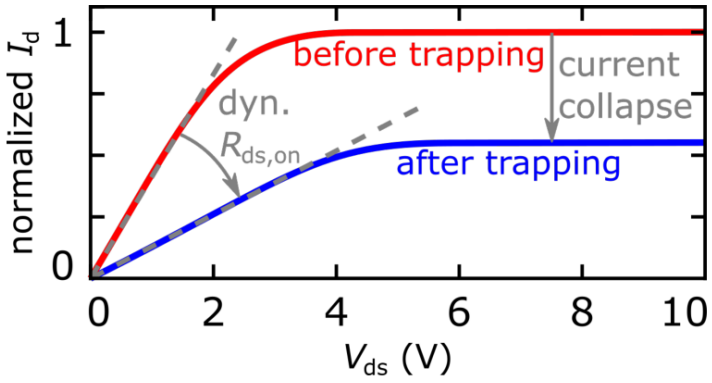


Figure 2.3: Effects of current collapse and dynamic $R_{ds,on}$ on the drain current with respect to the gate source voltage [KŤ20].

Dynamic effects like current collapse and dynamic on resistance $R_{ds,on}$ influence the drain current, as can be seen in Figure 2.3. These two effects can be attributed to trapping effects in the buffer or the surface of the device.

In contrast to the electrical mechanisms mentioned above, this thesis will focus on mechanical and thermal failure modes in the regime of robustness and reliability. The physical properties leading to these failure modes will be discussed in Chapter 3.

2.2 Methods and tools

2.2.1 Finite element method

Finite Element Method (FEM) is a general mathematical method to solve Partial Differential Equations (PDEs) approximately. These PDEs can be written in their differential (strong) form or in the integral form also called weak form. After reformulating the problem into the weak form the next step is the discretization. The discretization is done by discreting the volume in small finite elements, forming a mesh over the whole volume. The points within these elements, on which the PDE is solved are called nodes. Within one such element the exact solution is approximated by a function called shape

function. The combination of all these polynomial functions over all elements represents the approximated solution in the end.[1] After the discretization a set of matrix equations needs to be solved using well-known theories of matrix algebra.

Since FEM is used as tool in this thesis, from a practical point of view a Finite Element Analysis (FEA) consists of:

- **Abstraction of the problem:**
  In this step the object to model and the physics to include are determined.
- **Geometry construction:**
  The object under investigation has to be drawn in a Computer-Aided Design (CAD) program. Depending on the type of analysis a 2D model can be sufficient, or a 3D model is necessary.
- **Meshing:**
  Meshing is the step, setting the spacial points where the PDE is numerically solved. In general the number of points is higher in areas of bigger interest or where it is important to capture the exact geometry. In regions of lower interest the density is sparse.
- **Material assignment:**
  All elements formed in the meshing step need to be assigned a material, providing data for the type of physics incorporated in the simulation. For example in a pure thermal simulation the density, thermal conductivity and the specific heat are necessary to solve the heat equation.
- **Solution:**
  FEM problems can be solved in a transient or steady state. The Degrees of Freedom (DoFs) per spatial point are set by the physics (and the according PDEs) incorporated. The number of nodes in combination with the number of DoFs per point gives the overall number of DoFs in the system.
- **Analysis and Interpretation:**
  After solving the system, the critical task of assessing the results has to be done manually. If necessary, the improvements to the model are identified and the process is restarted.

As the software tool of choice in this thesis ANSYS Mechanical Version 18.2, from ANSYS situated in Canonsburg was used. It offers support in all steps, mentioned above, of a FEA. ANSYS Mechanical offers a scripting language Ansys Parametric Design Language (APDL) to design highly versatile models.

[1] Depending on the polynomial order of the shape function, elements are called linear or quadratic.

2.2.2 Laser scanning Doppler vibrometer

A Laser Scanning Doppler Vibrometer (LSDV) is a measuring instrument to gauge the movement of a surface. In principle, a LSDV is an interferometer with a measuring (test) and reference arm, as can be seen in Figure 2.4.

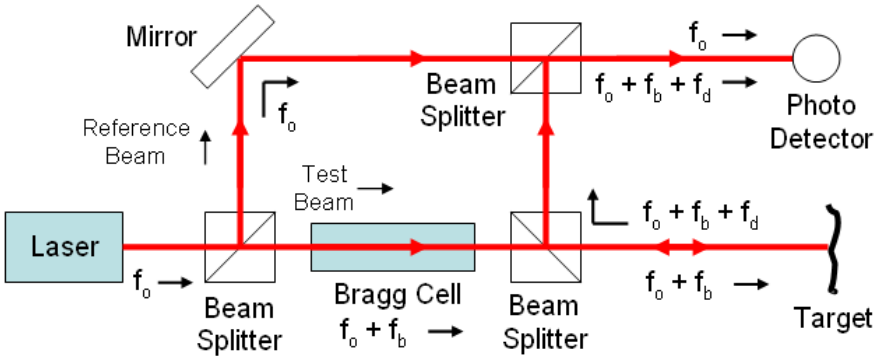


Figure 2.4: Measuring principle of an LSDV [Lad08].

Light from the laser is split in two, by the first beam splitter. The measuring beam is directed on the surface of the device under test (DUT) (named target in Figure 2.4). Due to the nature of the Doppler effect, reading as

$$f_d = 2 \cdot v \cdot \frac{\cos(\alpha)}{\lambda}, \tag{2.1}$$

a shift in the frequency f_d of the light occurs due to the velocity v of the reflective object. The parameter λ denotes the wavelength of the incoming light and α the angle between the velocity vector and the incoming light. Combining the reference beam and the measuring beam gives a beat frequency that is measured by the photo detector. The measured beam contains the frequency modulated velocity on the carrier frequency of the Bragg cell. The Bragg cell in the measuring arm adds an additional frequency f_b . This is done to switch from a homodyne regime to a heterodyne regime, which allows higher gains in the receiver. Via demodulating, it is possible to measure the velocity of the moving object. Integrating the velocity over time results in the required displacements. Two mirrors make it possible to move the measuring laser beam electrically over the surface, which denotes the scanning in LSDV.

The actual used LSDV was a Polytec PSV-400 [Pol20]. This instrument consists of a base tower, housing most of the electronic, and a scanning head, which is quite compact. The scanning head houses the interferometer part, which can be placed close to the

object to scan. Since normal optics with lenses can be used for the measuring beam, it is possible to measure objects of any size from full cars to microelectronics chips. This makes it a very versatile measuring instrument.

The combination of the LSDV and a function generator in the PSV-400 enables to synchronize the measurement with the excitation of the system. All these features can be utilized with a measurement software on a PC.

Evaluation of the extracted raw data (velocity) is done externally in a general programing language to ensure full control of the applied methodology.

2.2.3 Python

Python was the programming language of choice in this thesis due to its easy and user friendly syntax. It is an open source tool with an incredible amount of libraries providing functions ranging from basic vector operations (numpy) to complex numerical algorithms (e.g. for peak detection and fitting) in scipy [Ros95].

Chapter 3

GaN specific phenomena

This chapter will explain the thermal and mechanical properties of Gallium Nitride (GaN) and their interaction with each other. GaN is brittle material which features two stacking possibilities both resulting in spontaneous polarization. One possibility, Wurzit, features the crystal class $P6_3mc$. Crystals of that class feature spatially different centers of positive and negative charges and therefore feature the mentioned spontaneous polarization. This results in to two different effects, namely pyroelectricty and piezoelectricity, which will be explained thoroughly below. Furthermore GaN devices features also much better thermal capabilities over conventional Silicon (Si) devices, which will be discussed in this chapter.

3.1 Shifted thermal limits

Si devices suffer from a thermal instability above a certain temperature called thermal runaway. This phenomenon can be explained, following Stout [Sto06], by looking at the device and system reaction to temperature changes.

Figure 3.1 shows an explanatory stability diagram of a thermal system. It consists of two lines, representing the device and the system. The system line describes the thermal system around the device with the formula:

$$T_J = Q_{dev} \cdot \theta_{Jx} + T_x \tag{3.1}$$

where T_J is the junction temperature, Q_{dev} the device's power dissipation, θ_{Jx} the steady state thermal resistance of the system and T_x the thermal ground temperature of

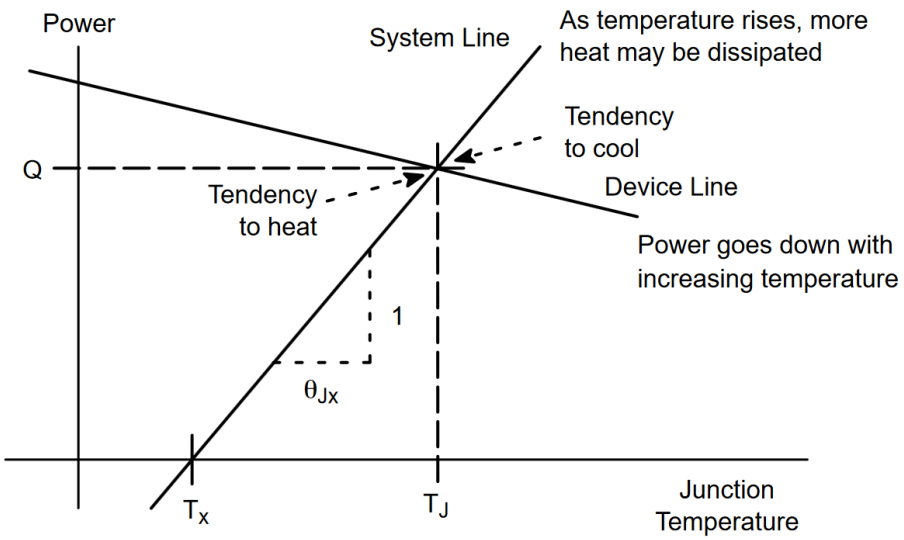


Figure 3.1: Example stability diagram of a thermal system. [Sto06]

the system. Rearranging Equation (3.1) and derivation of temperature yields the systems reaction to changes of the device temperature.

$$\frac{\mathrm{d}Q}{\mathrm{d}T_j} = \frac{1}{\theta_{Jx}} \tag{3.2}$$

It can be clearly seen in Equation (3.2) that if the temperature rises the system is able to evacuate more heat. This can be easily understood looking at Fourier's law,

$$q = -k\nabla T \tag{3.3}$$

where the rate of heat flux q depends linearly on the temperature difference. This represents typical thermal behavior of a system.

The device line in contrast describes the device's reaction of power dissipation with respect to temperature. In Figure 3.1 it can be seen that this device responds with reduced power output when temperatures rise. Depending on the temperature this is not the case for Si devices. Above a certain temperature, in short circuit, charge carriers

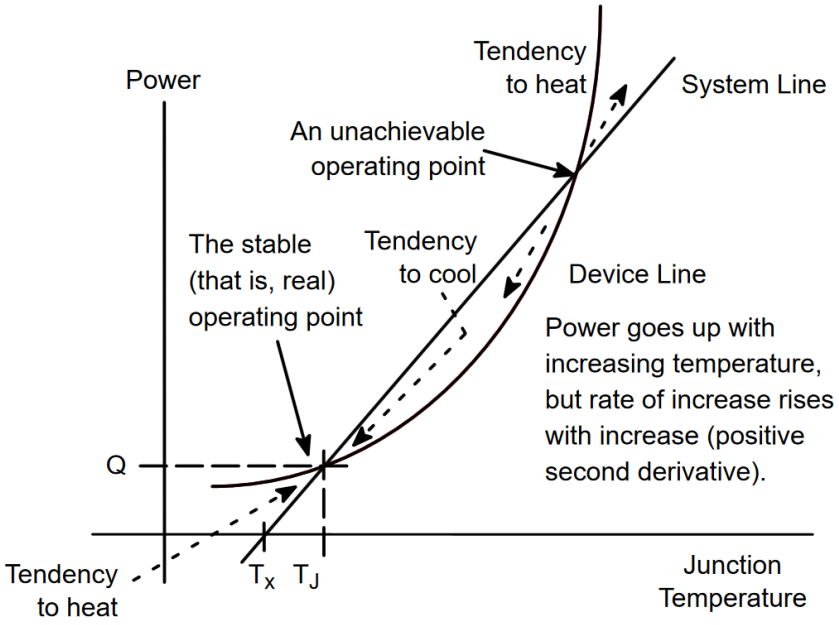


Figure 3.2: Overview of an thermally unstable system. [Sto06]

introduced by doping are increased by temperature and therefore the system will dissipate more power with rising temperatures resulting in a situation like Figure 3.2.

The exponential behavior the device in Figure 3.2 has, creates two intersections of the device and system line. The intersection at lower power is the stable operation point. Deviations to lower power and temperatures result in the complete system heating up again, whereas an increase in power and temperature not further than the second intersection will result in a decrease of both quantities back to the stable operation point. If the systems get pulled away from the stable point towards higher temperatures further than the second intersection, the system will not stabilize again. Beyond this point the device line has a higher derivative than the system line. Eventually thermally generated carriers will exponentially outmatch doping-defined carrier concentration, and therefore result in the device dissipating more additional energy than the system can dissipate due to the higher temperature difference. The outcome of this behavior is an uncontrolled heat up leading to the thermal destruction of the device. This phenomena is called thermal runaway and depends not solely on the materials used but also on the semiconductor technology used. For Si a thermal runaway temperature in the range of 300 °C to 600 °C is typical, whereas GaN features significantly higher runaway temperatures [But+11]. When subjecting a Si semiconductor to high temperatures or extensive loads, thermal runway will trigger the first (thermal) failure mechanism destroying the device and covering possible failure mechanism at higher temperatures. Since in GaN High Electron

Mobility Transistors (HEMTs) the charge carriers cannot be thermally created, resulting in a flatter device line, the thermal runaway happens at much higher temperatures. This opens the possibility of high temperature application with GaN, but making it necessary to investigate high temperature failure modes. This will be done extensively in Chapter 4.

3.2 Piezoelectricity

Piezoelectricity is the ability of a substance to react to mechanical stress with a charge separation (voltage). The vice versa effect, where a voltage is applied to a substance and the material deforms is subsequently called reverse piezoelectric effect.

Piezoelectricity is the result of the dependence of the center of positive an negative charges created in 21 crystal classes, if they are subjected to mechanical strain. 10 out of this class, called polar, even feature spontaneous polarization, which means that they show a electrical dipole even without being subjected to mechanical strain.

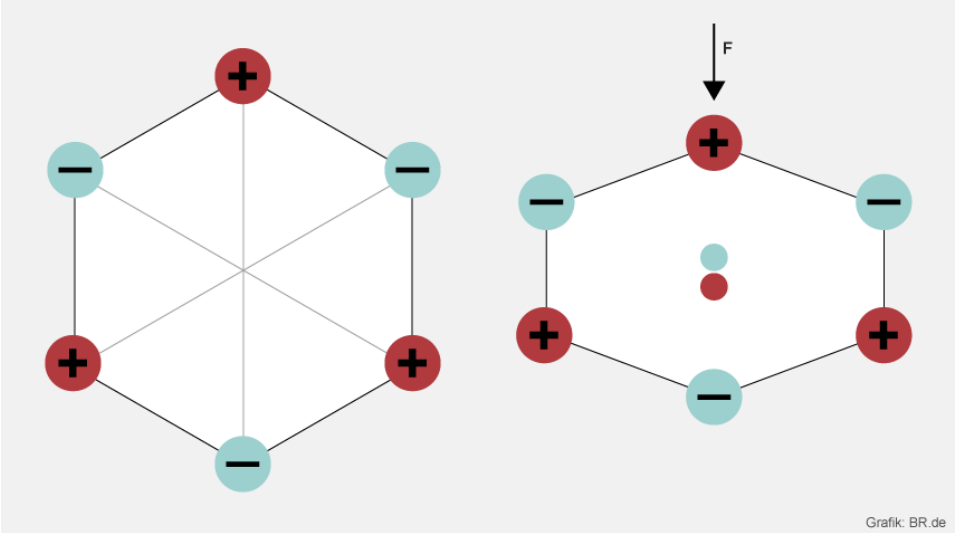


Figure 3.3: Stability diagram of a Si device. [BR17]

Figure 3.3 shows the crystal lattice and the center of positive and negative charge. It can be seen that if the lattice is deformed by the vertical forces the positive and negative centers increase the spatial distance between them. Taking the definition of an electric dipole moment p of

$$\vec{p} = q \cdot \vec{d}_q \tag{3.4}$$

with q as charge and d_q the distance between the charges. It can be easily understood why a deformation results in an electric dipole. The governing equations of piezoelectricity in the strain-charge form in Voigt notation are [Ike96]:

$$\begin{aligned} \boldsymbol{S} &= s^E \boldsymbol{T} + d_{piezo}^T \boldsymbol{E} \\ \boldsymbol{D} &= d_{piezo} \boldsymbol{T} + \epsilon_0 \epsilon_r \boldsymbol{E} \end{aligned} \tag{3.5}$$

, where d_{piezo} are the piezoelectric matrix coefficients, $\boldsymbol{S}$ is the strain vector whereas $\boldsymbol{T}$ denotes the stress vector. s is the mechanical compliance matrix at zero electric field and $\boldsymbol{D}$ is the electric displacement.

Naturally occurring crystals featuring piezoelectricity are for example Quartz [Car67] and even sucrose (sugar) [New05] with piezoelectric coefficients d in the range of $-2.3\,\mathrm{pC/N}$ to $-4.22\,\mathrm{pC/N}$. For technical applications synthetic ceramics like barium titanate ($BaTiO_3$) or lead zirconate titanate ($PbZr_xTi_{1-x}]O_3$) (PZT) are used ($270\,\mathrm{pC/N}$ to $580\,\mathrm{pC/N}$). They feature high piezoelectric constants making them a good choice for sensors, actuators and other wide fields of different applications. The piezoelectric properties and its implications are discussed in Chapter 5.

3.3 Pyroelectricity

Pyroelectricity is the ability of a substance to react to heating or cooling with a temporary charge separation (voltage) (see Figure 3.4).

This initially leads to the formation of surface charges that are perpendicular to the polar axis of the material. Compensating charges from the environment ensure the charge balance at constant temperature.

This phenomenon is closely related to piezoelectricity. This can be understood by looking a the crystal classes which feature pyroelectricity. Out of the 32 crystal symmetry classes the 10 polar ones, mentioned also in Section 3.2, feature pyroelectricity. Pyroelectric material are used for example in infrared detectors, particle accelerators and energy harvesters [AB13].

Pyroelectricity is mathematically described as:

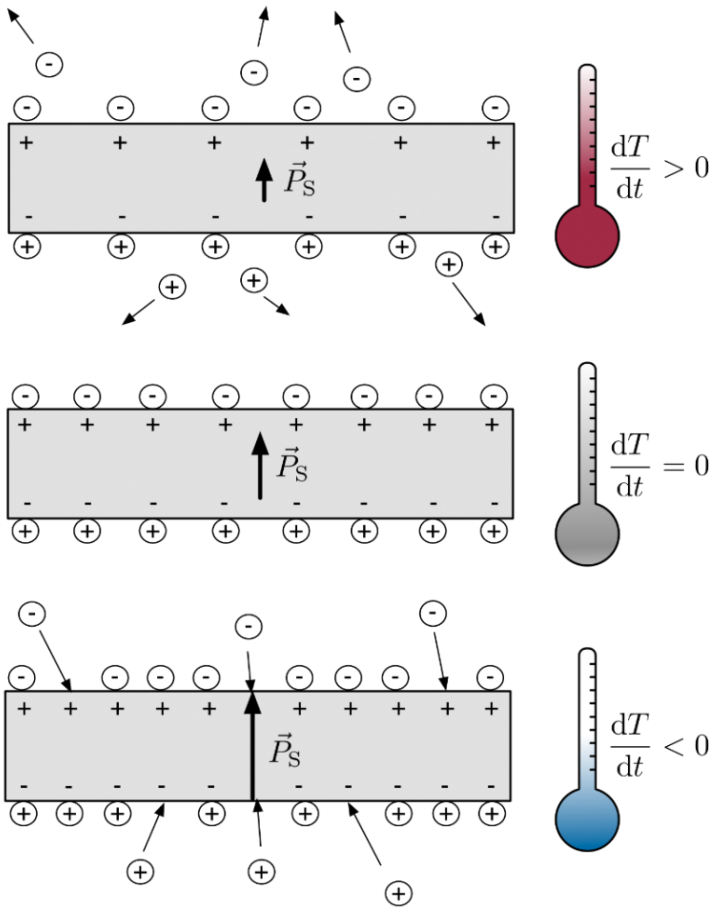


Figure 3.4: Principle of pyroelectricity [Fre20]. In the middle picture a pyroelectric material in thermal equilibrium can be seen. To compensate for the polarisation, surface charges ensure charge balance. If the material is subjected to a temperature change, the polarisation changes due to the changed distance between the positive and the negative charge center. The change in surface charges for charge balance can be measured as current.

$$p_{pyro} = \frac{\partial P}{\partial T} \tag{3.6}$$

where p_{pyro} denotes the pyroelectric coefficient, P the polarization and T the temperature.

Following [Byk+96] the pyroelectric coefficient p is in the range of $0.85\,\mu C/(K\,m^2)$ in GaN. An estimation of the size of this effect can be done by calculating the voltage which a temperature rise would yield in typical HEMT dimensions. Treating the charge on

the surface of a block of GaN as plate capacitor makes it possible to come up with an estimation. The voltage U in plate capacitor is defined as:

$$U = E \cdot d_{cap} \tag{3.7}$$

,where E is the electric field and $d_{cap}$the distance between the plates. The electric field can be written as:

$$E = \frac{\sigma_q}{\epsilon_0 \cdot \epsilon_r} \tag{3.8}$$

, where σ_q is the charge area density and ϵ_0 ϵ_r the natural and the specific dielectric constants of the material between the plates. This leads to

$$U = \frac{p \cdot \partial T \cdot d_{cap}}{\epsilon_0 \cdot \epsilon_r} \tag{3.9}$$

which yields roughly 32 mV for a typical situation found in a GaN HEMT in line with [SBG98]. The temporarily occurring voltage is therefore four orders of magnitude away from typically applied voltages and can therefore safely be neglected.

3.4 Interaction electric field temperature

As can be seen in the Heckmann diagram in Figure 3.5 the effects of piezoelectricity, pyroelectricity and thermal expansion connect the mechanical and electrical properties.

It was discussed in Section 3.3 that the pyroelectric effect can be safely neglected due to its size. This can lead to the wrong perception that the stress field is independently influenced by the temperature and the electric field. Even though the pyroelectric effect is neglected, following [Pri16] it can be shown that the applied electric field and the temperature field are still interacting. This means that the resulting stress field of

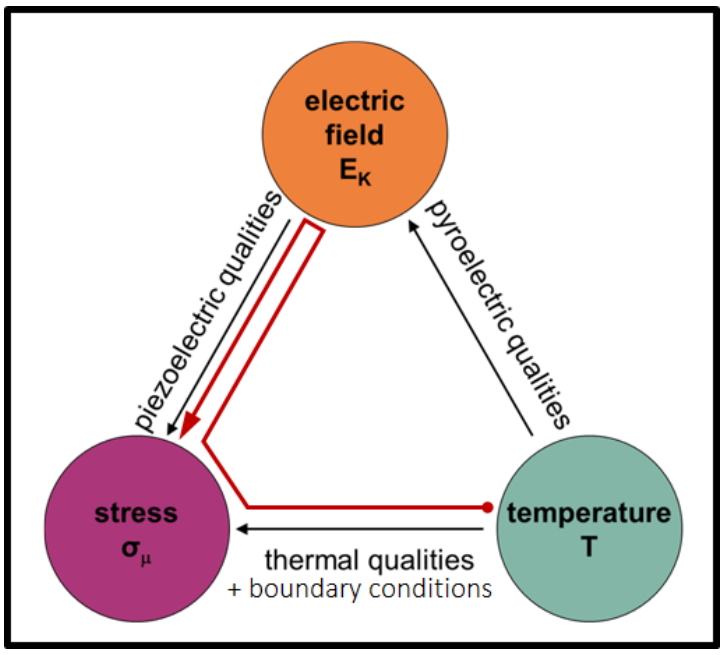


Figure 3.5: Heckmann diagram

temperature and electric field applied at the same time it is not a superposition of the pure temperature stress field and the pure electric field stress field.

The interaction taking place is shown in Figure 3.5 marked by the red arrow. The temperature in the block causes a stress state in the assembly, due to thermal expansion in conjunction with the boundary conditions. This stress via the piezoelectric effect causes an electric field which in return interacts with the stress field.

To asses the strength of this effect a sample brick in the typical dimensions found in GaN HEMTs is used to investigate.

In Figure 3.6 a thin GaN layer on a silicon block is shown. In the first step the GaN layer is subjected to vertical field between the electrodes with 600 V depicted in Figure 3.7(a). The second independent step involves the full block being subjected to a temperature change from 293 K to 473 K seen in Figure 3.7(b).

Since we are working with linear elastic material model, following Hooke's law (Equation (3.10)) there is no difference between adding stress σ_{mech} or strain ϵ_{mech}.

$$\sigma_{mech} = E_{mech} \cdot (\epsilon_{mech} - \alpha_c \Delta T) \tag{3.10}$$

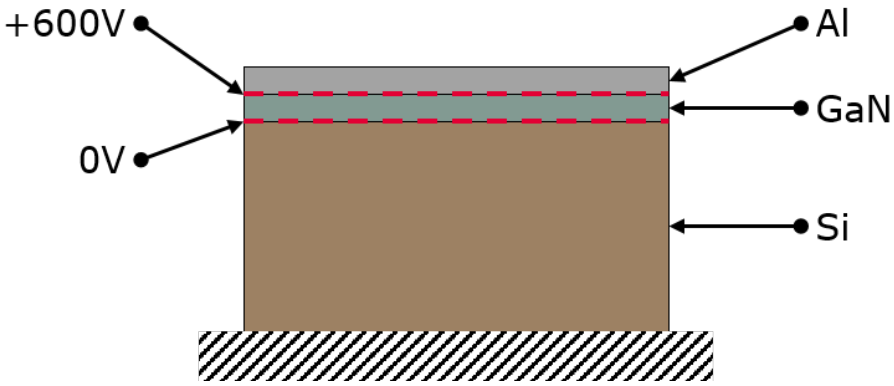
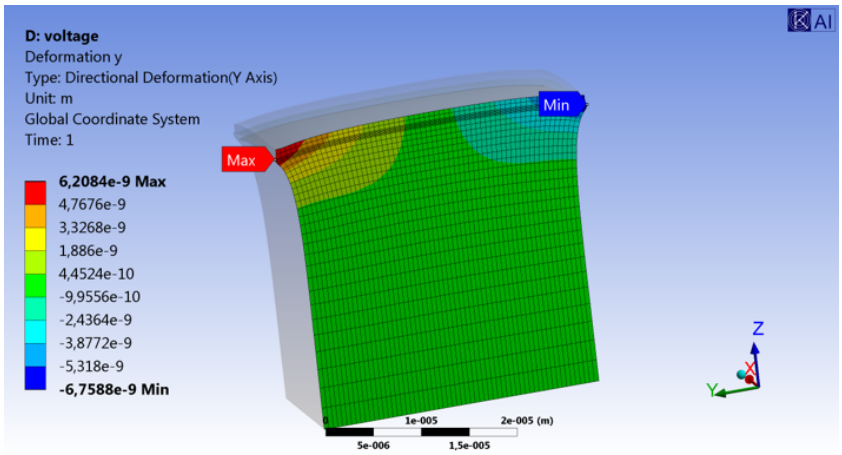
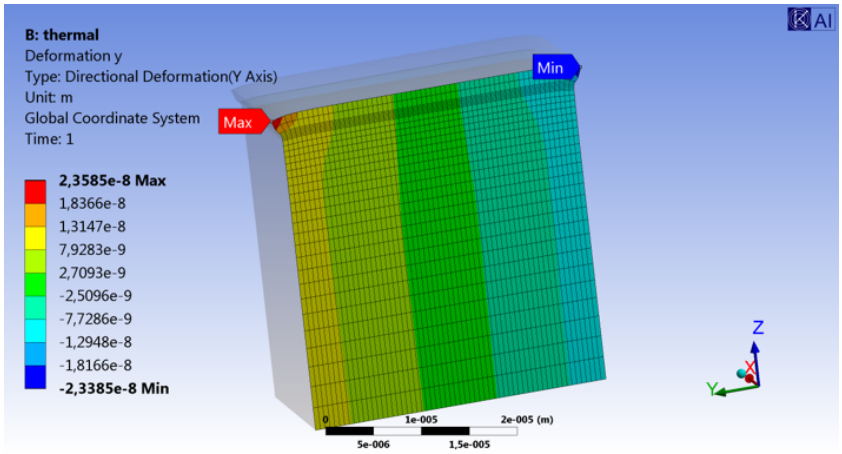


Figure 3.6: Stack to show the interaction of temperature and voltage.



(a) y direction deformation of the stack is subjected to a homogeneous electric field.



(b) y direction deformation of the full stack (relaxed at 293 K) is subjected to temperature increase ΔT of 180 K

Figure 3.7: Reaction of the test block to temperature and voltage.

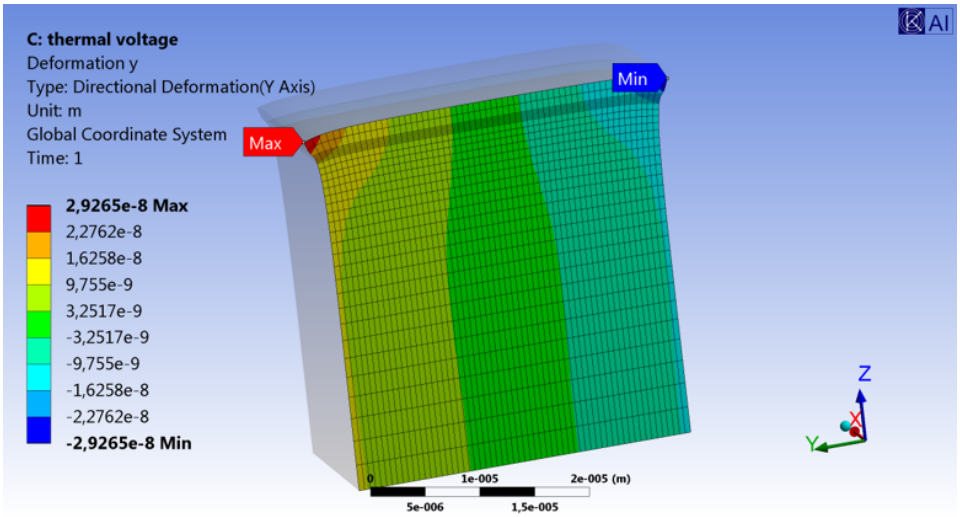


Figure 3.8: y direction deformation of the stack subjected to the temperature change and the voltage at once.

In difference to the two independent steps, a simulation where the voltage and the temperature are applied together is also conducted, seen in Figure 3.8.

The deformation field of the pure voltage simulation added to deformation field of the pure temperature field and then compared to the combined simulation approach.

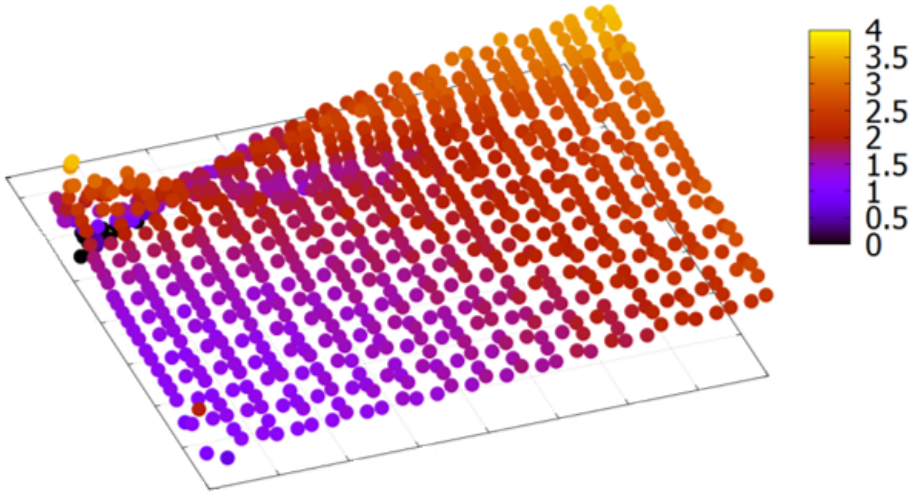


Figure 3.9: Relative difference in percent between the superposition of deformation fields of voltage and temperature separately and the combined approach.

As can be seen in the relative difference in percent in Figure 3.9 the difference is below 4 %. This illustrates that there is an interaction effect on the stress field when the block is subjected to temperature change and electric field at the same time.

Due to the small value of this combined effect in a typical GaN HEMT scenario the combined effect can be safely neglected. To neglect this makes it possible to study temperature effects and piezoelectric effects separately.

Chapter 4

Short thermal pulses (aluminium protrusion)

Gallium Nitride has, as already shown in Chapter 3, a significantly higher run away temperature compared to silicon. In common silicon devices the device performance is limited in short thermal pulses by the temperature in the silicon. Since this limit is much higher in Gallium Nitride (GaN), the question of the mechanism that triggers failure in GaN based High Electron Mobility Transistors (HEMTs) arises. For investigation, an appropriate test setup to thermally stress the chip as much as possible in a very short time, was required. A test condition is necessary such that internal temperatures around the thermal runaway temperature of silicon semiconductor devices can arise. It is known from simulations that a heatwave in GaN roughly travels $5 \times 10^{-6}\,\mathrm{m}$ in $250 \times 10^{-9}\,\mathrm{s}$, a result obtained by the estimation of the speed of the heatwave [MVD16]. This is just possible in a hyperbolic heat equation (also known as the telegraph equation in literature), since in the commonly used parabolic it is not possible to deduce a heat wave speed:

$$-\frac{1}{u^2}\frac{\partial^2 T}{\partial t^2} - \frac{1}{\alpha_{therm}}\frac{\partial T}{\partial t} + \nabla^2 T = 0 \tag{4.1}$$

where T represents the temperature, α_{therm} the thermal diffusivity, τ the characteristic time of the temperature build up and $u = \left(\frac{\alpha}{\tau}\right)^{\frac{1}{2}}$ is considered [NOR94]. By using the characteristic value of thermal diffusivity, which is in the range of $43 \times 10^{-6}\,\mathrm{m^2/s}$ [LRS01] and a τ of $100 \times 10^{-9}\,\mathrm{s}$ yields a rough estimate of the velocity of a heatwave of $\sim$20 m/s, which is in line with the simulation results mentioned above.

To stress the chip in very short time with high temperatures, a high power density needs to be present within the chip, which is the reason why a short circuit test setup was

chosen. The device used to investigate this thermal overload behavior was a normally-off GaN HEMT. The device featured an $R_{ds,on}$ of 70 mΩ and was packaged in a DSO-20 package. This chip features a normally-off behaviour realized by a p-GaN gate structure. The pulses used to stress the chip were outside the Safe Operating Area (SOA) of the chip and were aimed to determine principle physical limits. The characteristic SOA diagram for this GaN chips is shown in Figure 4.1.

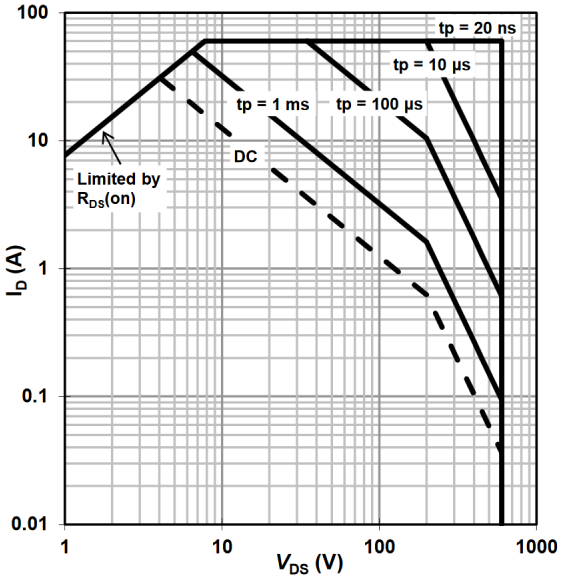


Figure 4.1: Principle SOA diagram of GaN HEMTs [18]. The SOA depends on the time of the pulse. For pulses with a duration of approximately 100 µs, the applied V_{DS} and I_D are at least one order of magnitude away from their rated limits.

In the following sections it will be shown how the chip was stressed and which physical failure analysis were done. Additionally, the findings from simulation, which were done to understand the provoked failure mode, are summarized. At this point note that the main findings are already published in a conference proceeding paper of the WOCSDICE conference [Pri+17b] and an article in the Microelectronics Reliability journal [Pri+17a].

4.1 Measurement setup

The used test bench, schematically illustrated in Figure 4.2 was provided by the lab personal at Infineon technologies in Villach. In principle the setup puts the device under test (DUT) in short circuit condition and records the corresponding power dissipation by the drain source voltage V_{DS} and its corresponding current I_D.

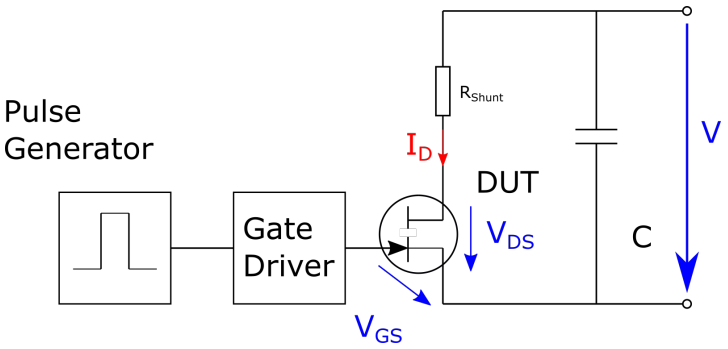


Figure 4.2: Circuit layout of the stress test bench.

To be more precise, the test bench connects a signal generator with a gate driver that operates the DUT. By means of a trigger the pulse generator generates a rectangular pulse, which switches the transistor in the on-state. The corresponding voltage V_{GS} is directly set by the voltage of the pulse. At this point it is important to know that the DUT can be supplied with two different V_{DS} voltages, 400 V and 600 V. The current I_D is defined by the values of V_{GS}, according to the transfer characteristics.

The capacitor shown in Figure 4.2 consists of several close by ceramic capacitors in order to provide a low inductance, and a bank of foil capacitors, which provides the energy needed within the pulse. This setup is necessary to supply the power needed during the pulse. With a small precision resistor R_{shunt} the current across the HEMT I_D can be converted into an voltage signal and measured by an oscilloscope. For easier preparation and modularity, the DUT was soldered on a separate printed circuit board (PCB), which can be easily plugged into the main board. The complete test board can be seen in Figure 4.3. Lastly the setup was placed inside a High Voltage (HV) housing for safety reasons.

Different values of drain currents I_D at the two mentioned different levels of drain source voltage V_{DS} were used to stress the chip. After stressing, two different failure modes could be clearly distinguished, when comparing the failed DUTs. Stress conditions at V_{DS} 400 V or 600 V with drain currents I_D lower than 10 A failed into a permanent off-state. This causes the device to switch off even though V_{GS} is still applied. On the contrary, chips stressed with V_{DS}=600 V and currents I_D higher than 10 A led to failures with a permanent on state, resulting in the complete destruction of the DUT. Since no fail safe circuitry was placed in the circuit design to protect the chip, no physical failure analysis could be conducted for this failure mode. Independent investigations by Infineon revealed the second failure mode to be rooted in the device properties and parasitic effects of GaN device [Hua+14], rather than in thermal and thermo-mechanical phenomena. Such device behavior is explicitly not part of this thesis, and we focus

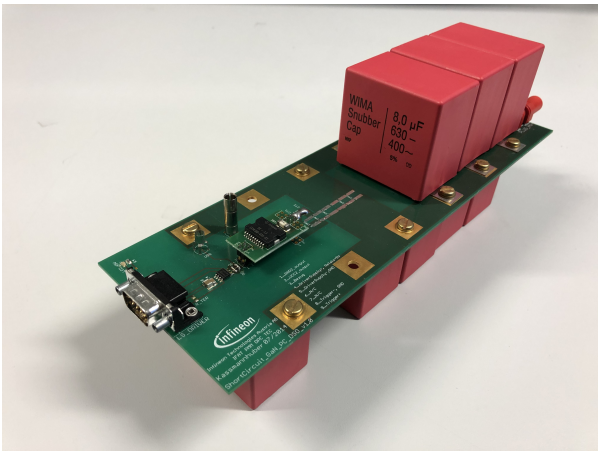


Figure 4.3: Realized implementation of the test bench in laboratory.

instead on mechanism one. The failure mode of interest is an off state caused by a permanent short between gate and source, linked to the first combination of drain voltage and current. A typical short circuit pulse, provoking the mentioned off state failure mode is represented in Figure 4.4.

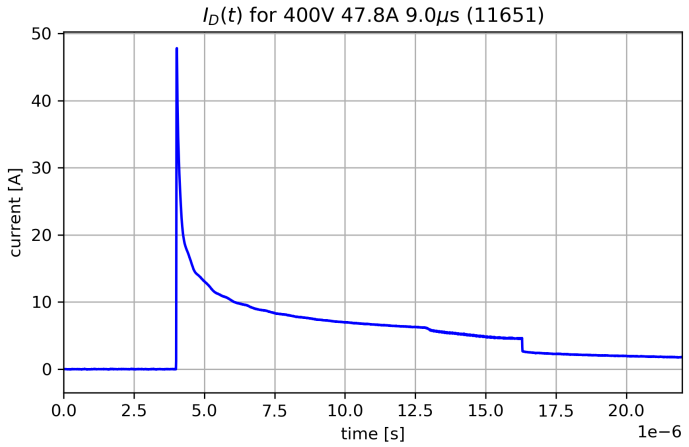


Figure 4.4: Exemplary $I_D(t)$ of a sample short circuit pulse for a constant V_{DS} of 400 V. V_{GS} was held for 1 ms. As can be seen the short between gate and source forces the device in an off state much earlier.

4.2 Model

The model used to investigate the off state failure mode is a 2D plane stress model (describing a single cell of the GaN chip), which incorporates for thermal and mechanical

physics. An overview of an actual GaN chip is shown in Figure 4.5, where a single cell is marked in red.

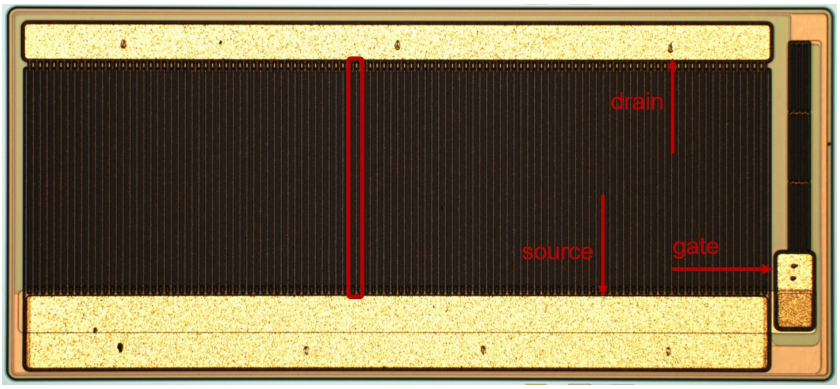


Figure 4.5: Topview of a GaN HEMT, with highlighted drain, source and gate pad. The red rectangle shows one single cell. The complete chip measures $4.8 \times 2.2\,\mathrm{mm}$

Looking at Figure 4.5, it can be seen that the source bond pad is on the bottom and the drain pad is on top. On the right hand side the bond pad for the gate can be seen. The chip itself consists of many single cells stacked in parallel to meet the current requirements of the product. The source, drain and gate lines stretching inwards to the chip are called fingers. Due to the small geometric features within a single cell, required to be spatially resolved, it is not possible to simulate the whole chip in three dimensions. For that reason, a single cell model, as shown in Figure 4.7, was constructed.

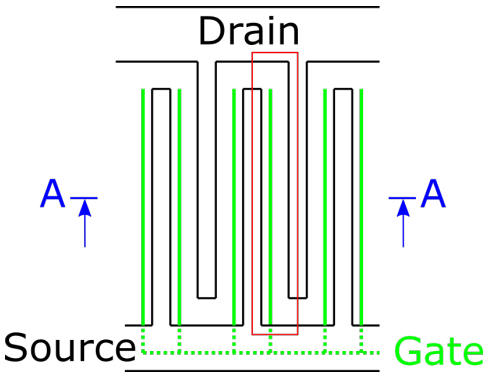


Figure 4.6: Schematic top view of a GaN HEMT, with highlighted drain, source and gate. The red rectangle marks one single cell. The neighbouring single cells show an antiparallel alignment. The gate bus, connecting all the gate fingers is below the big source pad on the bottom.

Within this cell the source can be seen on the left and the drain on the right. In the full chip these single cells are stacked in an antiparallel, parallel manner so that the source or drain from the next cell touches with the previous. The connection of the

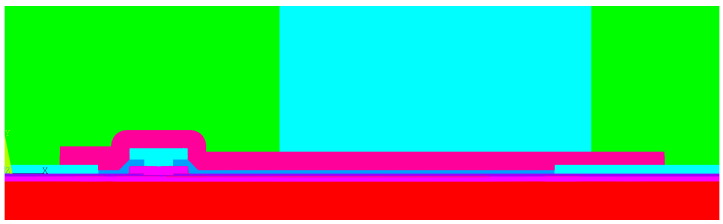


Figure 4.7: Model of a single GaN cell (section view AA from Figure 4.6). The source is located on the left, whereas the drain is the right. The colors mark different materials.

gate cannot be seen in the 2D cell because it runs under the source field plate and is routed to the surface at the beginning of the gate finger. The complete model is far more extensive to the top and to the bottom to avoid thermal boundary conditions, which would result in more parameters to be properly determined. To be more precise, the chip is modeled to such a geometric extent that the heatwave cannot reach the adiabatic boundary condition. The complete set of boundary conditions is discussed in Section 4.3.

The GaN HEMT is built in a gallium nitride on silicon technology. As pointed out in the previous chapters this structural approach results in the need of an adaption layer between the GaN and the silicon substrate. The used superlattice structure was not explicitly modeled in this thesis, but a homogenized layer was used instead. The used thermal values of the homogenized material were measured by a cooperation partner within the PowerBase project on the actually used material. Figure 4.8 shows a schematic of the model and the used materials.

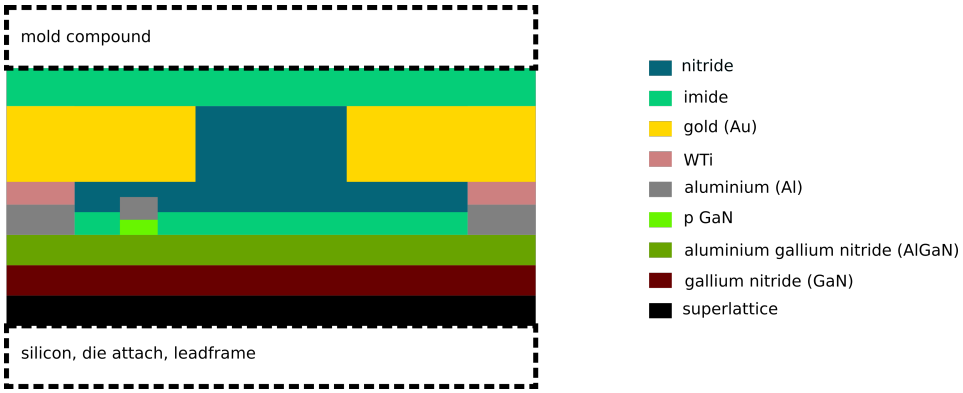


Figure 4.8: Schematic (not in scale) of a single GaN cell and the materials used.

The accuracy of the geometric features of the model is varied over the single cell. Closer to the two-dimensional electron gas (2DEG) the level of detail was chosen very high, with resolutions of 20 nm, whereas further away from the heat source the detail grade was lowered. In a thermal Finite Element Method (FEM) model, which solves

the heat equation, the volumetric mass density ρ, the heat capacity C and the thermal conductivity k are needed. Table 4.1 lists all the used material data. If the physical properties vary over temperature just the value for room temperature is explicitly listed.

Table 4.1: Thermal properties of all used materials. (most values are taken from [Cve+02], the rest are company internal measured values)

	density ρ ($\mathrm{kg/m^3}$)	**heat capacity** C ($\mathrm{J/(kg\,K)}$)	**thermal conductivity** k ($\mathrm{W/(m\,K)}$)
mold compound	2050	769	1
imide	1400	344	0.5
gold	19 300	129	315
aluminium	2689	921.1	237
p-GaN	6150	429.6	114.8
AlGaN	6011	537	50
GaN	6150	429.6	114.8
superlattice	4705	582	10
silicon	2358	706	74.8
die attach	3500	344	15
leadframe	8960	385	401

4.3 Thermal simulations

The first step in simulation to understand the failure mode, was a thermal simulation of the single cell. Keep in mind that the model as described in Section 4.2 is just a single cell of the complete chip. From the electrical measurement one can observe that the permanent off state is caused by an electrical short between gate and source. The spatial point within the chip where the short is caused can be found by Photo Emission Microscopy (PEM) (this is explained in more detail in Section 4.4). Considering the typical location in planar view of the chip, two conclusions can be drawn, which allow this radical simplification.

It can be clearly seen in Figure 4.9 that the typical failure spot is not on one of the edges of the chip, but more in the direction of the interior. This can be attributed to the fact that on the border the chip is not only cooled by the top and the bottom, but also by the sides by heat splay to the non active areas of the chip, which results in a lowered temperature in this region. Therefore, it is safe to assume that the failure mechanism is triggered in the middle (hot) area of the chip. This hot area can be imagined symmetrical

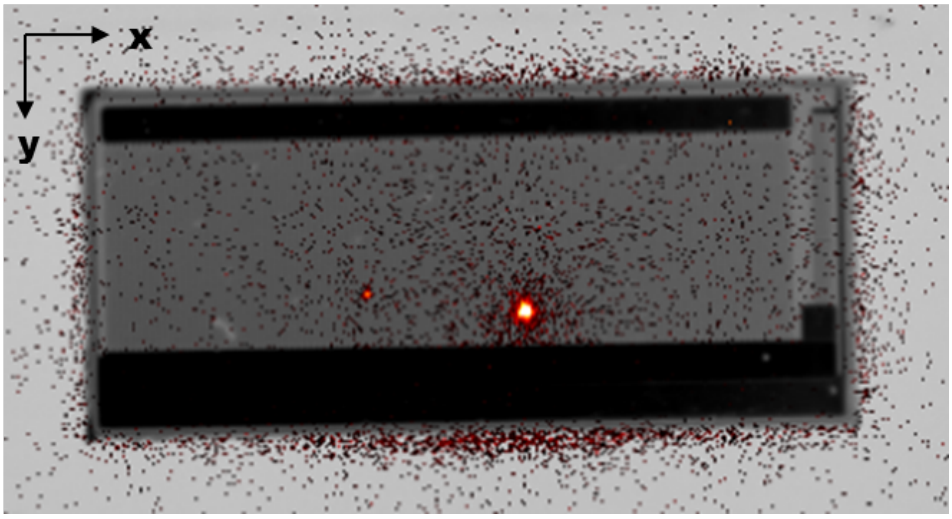


Figure 4.9: Overview of a GaN HEMT. On the top the drain pad can be seen and the source on bottom. The single small pad to the right is the gate pad.(compare with Figure 4.5) PEM performed at the failure analysis labs of Infineon makes it possible to determine the spot of the failure.

with respect to all borders. A second effect shifts this failure prone area closer to the gate bus (see Figure 4.6). As noted in the description of Figure 4.6, the gate fingers start from the bottom border of the chip and stretch upwards across the chip. This leads to a phenomenon called gate debiasing. The full gate voltage is just applied to the cell at the beginning of the gate finger, when the gate capacity is charged, since due to the resistance of the gate metal a small voltage drop occurs till the end of the finger. This leads to lower gate voltage at the end of the gate finger and therefore to a smaller current and heat dissipation at the beginning of the pulse. The combination of these two effects make the hottest region shift towards the start of the gate finger. Simulating a single cell with adiabatic boundary condition, accounting for no heat splash to the sides, and full gate voltage results in a cell in the hottest area of the chip.

4.3.1 Boundary conditions

The boundary conditions can be split in two. One restriction refers to the thermal behaviour of the model on its borders and the other one how energy is dissipated within the model. The model is created in such a way that on all borders adiabatic boundary conditions can be applied. Due to the fact that the chip exhibits a periodic parallel antiparallel structure, there is no net energy flow between single cells. This is reflected by adiabatic boundary conditions to both sides. Since the power of the chip is dissipated in the 2DEG in the middle of the chip, the heat wave has its origin there. This approach

avoids a potential source for errors in form of the convection boundary conditions on top and bottom (in z-direction) of the chip, the model was made spatially big enough so that the heat wave cannot reach the border of the model over the duration of one stress pulse. The necessary size of the model can be roughly estimated from an engineering approach, using the parabolic heat equation following [Mar10]

$$k\frac{\partial^2 T}{\partial x^2} = \rho C\frac{\partial T}{\partial t} \tag{4.2}$$

, with the characteristic length

$$l_{typ} = 2 \cdot \sqrt{\frac{k}{\rho C}t} \tag{4.3}$$

Then, for a typical short circuit pulse of 200 µs and the material properties of silicon it is possible to conclude that

$$l_{typ} = 2 \cdot \sqrt{\frac{74.8\,\mathrm{W/(m\,K)}}{2358\,\mathrm{kg/m^3} \cdot 706\,\mathrm{J/(kg\,K)}} \cdot 200\,\mu\mathrm{s}} \tag{4.4}$$

, yields a characteristic length of approximately 200 µm. This justifies also the use of adiabatic boundary conditions on top and bottom of the model, if the dimensions are big enough.

4.3.2 Heat generation

The heat generation rate is measured during the short circuit pulse by voltage and current, from which the power can be deduced. In contrast to literature [ABM12], where the heat dissipating volume is presumed to be very small at the gate edge facing the drain side of the chip, a Technology Computer-Aided Design (TCAD) simulation by Infineon showed a spatial distribution of the heat dissipation nearly along the full channel. The accurate modeling of the heat dissipation is necessary since we are not interested in an average channel temperature or the temperature of the lead frame, but in an accurate temperature field in and around the gate, where the failure originates. To get the correct spatial power distribution, several TCAD simulations were conducted, where the two drain source voltages V_{DS} were modeled with different gate voltages V_{GS} to get a range of drain currents. This makes it possible to understand the effects of increasing and decreasing drain currents on the spatial power distribution.

In the TCAD simulations the drain source voltage V_{DS} was kept constant and the drain current I_D was regulated via the gate voltage V_{GS}. As can be seen in Figure 4.10, the electric potential was plotted along the 2DEG in the single cell. Note that at the gate edge facing the drain side, the electric field and therefore the power dissipation is highest. The second peak in the electric field distribution is at the edge of the source field plate, which is used to smooth out the electric field. Interesting to see in Figure 4.11 is, that the position of the two peaks in the power distribution does not shift with the current level, but only the absolute values changes. To determine the average spatial shift of the power distribution with the drain current I_D, the power dissipation curves were normalized to 1 A and plotted against each other.

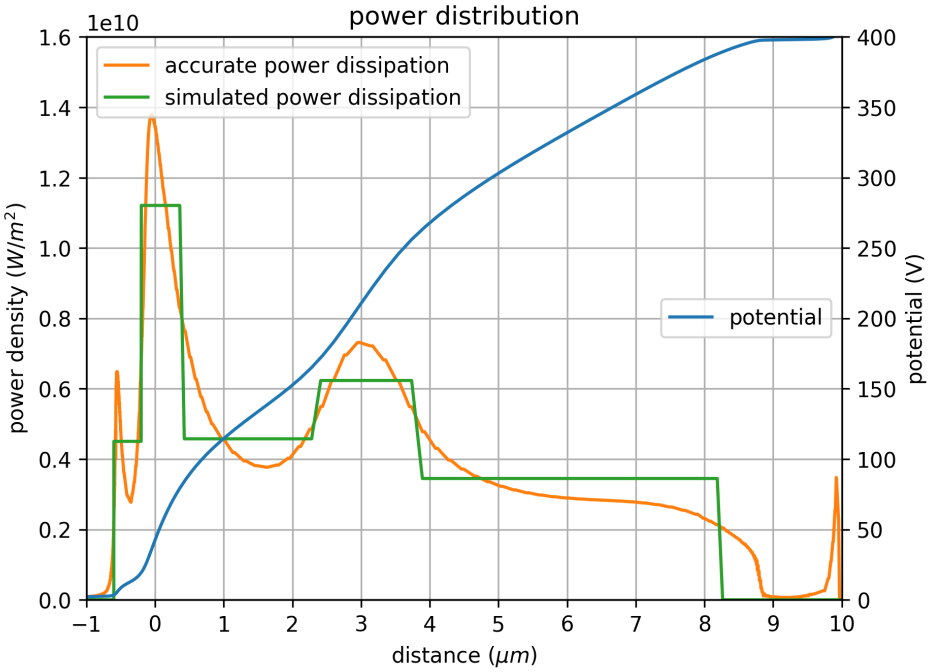


Figure 4.10: Power dissipation and electric potential across the full cell. Distance 0 depicts the gate edge facing the drain side. Additionally the 5 areas and the over all averaged power can be seen in the step function. Note that this is an exemplary graph for 400 V and 27 A. The unit W/m^2 is from the simulation and is meant as Watt per chip area.

For simplification, the total area of power dissipation was split into five fixed areas capturing for the two peaks of the power distribution as well as the neighborhood. The power dissipation within these five areas refers to the average of the simulated spatial power distribution, where for different current levels, a corresponding averaged value is calculated. By plotting the averaged power levels against the current I_D, a linear regression can be fitted, seen in Figure 4.12. This regression gives the spatial relation of the power density with respect to the drain current for each area.

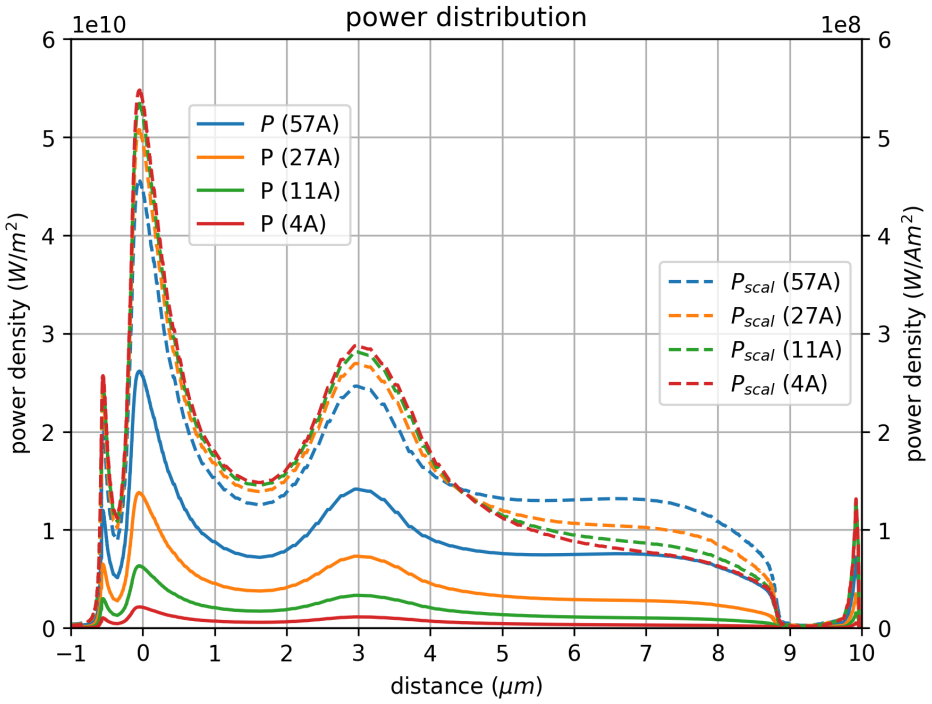


Figure 4.11: Power distributions for different current levels at 400 V. Additionally, also power per ampere is shown on the second y-axis.

Since V_{DS} is constant during a stress pulse, it is possible to assign a power level to each of the five areas according to the drain current by means of the above mentioned regression. This over all power dissipation characteristic accounts for two effects. It incorporates the decrease of the absolute power level due to self heating during the pulse (measured) (see Figure 4.4). Furthermore it accounts for the spatial shift of the power distribution due to the decreasing drain current.

These power distributions leads to temperature distributions exemplarily shown in Figure 4.13.

4.4 Advanced physical failure analysis

In addition to the numerical investigations by means of FEM, physical failure analysis was conducted to get deeper insights in the short circuit failure mechanism. The failure analysis was split into two parts. All preparation steps including the localization were done at the failure analysis lab of Infineon Munich. The following in depth analysis based

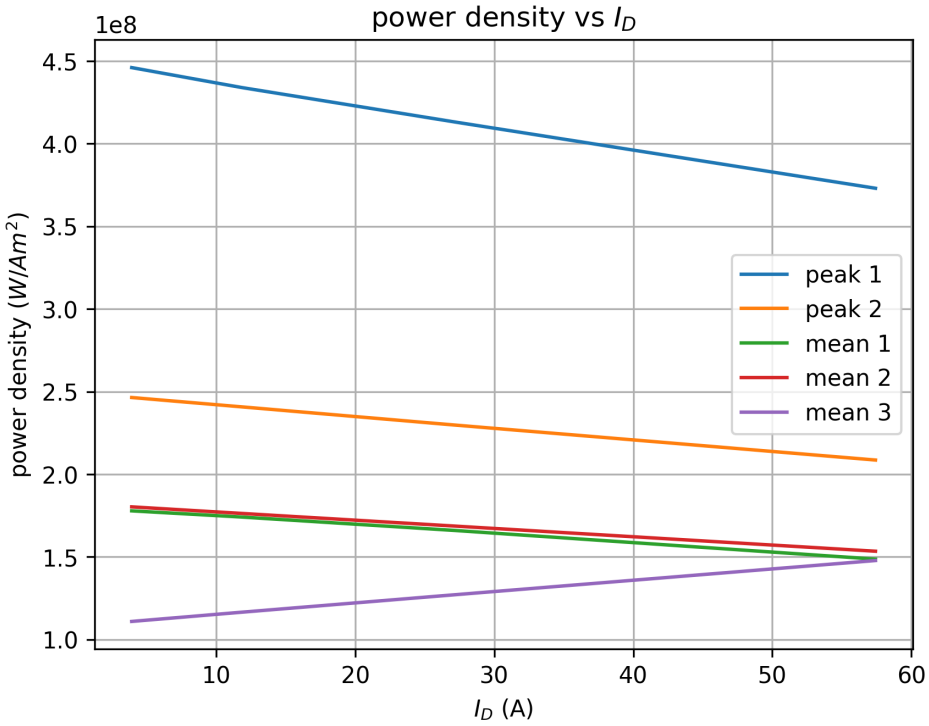


Figure 4.12: Linear regression of the power distribution in W/m^2 for different current levels at $V_{DS} = 400\,V$.

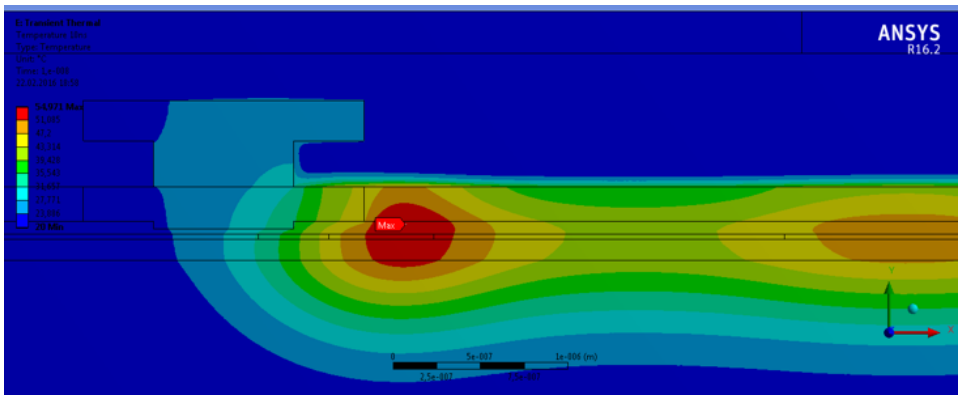


Figure 4.13: Exemplary temperature distribution at an arbitrary time within a pulse.

on Scanning Electron Microscopy (SEM) and Transmission Electron Microscopy (TEM) were done at IMWS Halle within the cooperation of the project PowerBase.

As described in Section 4.3, it is possible to detect a location of the short, between gate and source, from the backside of the chip. This is only possible if the chip is decapsulated and removed from the lead frame. After the removal of the lead fame the silicon substrate is completely removed and the superlattice layer and the GaN layer are thinned till

they get transparent. With this preparation it is possible to use PEM to localize the protrusion forming the short, see Figure 4.9. Focused Ion Beam (FIB) cuts furthermore make it possible to mill grooves into the chip to get a side view of the shorted gate finger. At the immediate vicinity of the point of failure SEM pictures were taken.

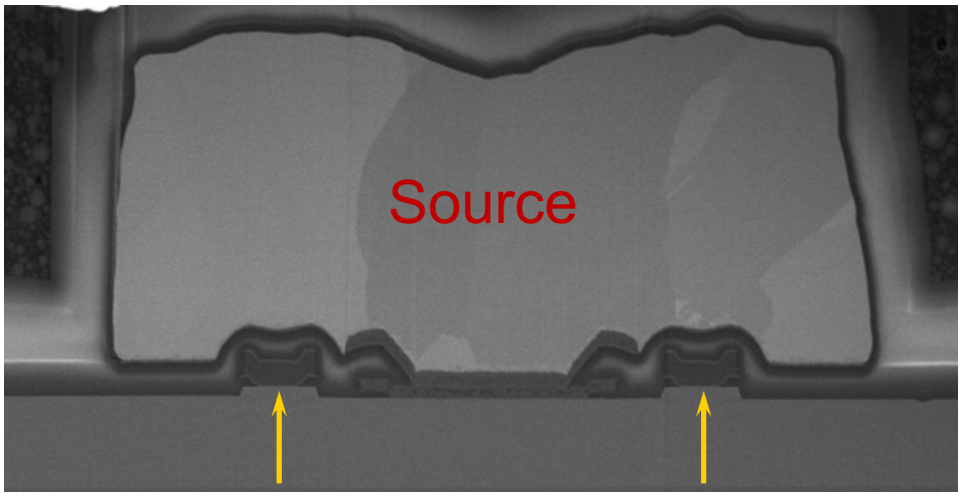


Figure 4.14: SEM picture of a cross section showing the gate source gate area of two single cells. The big source field plate in the middle is covering the gate fingers to the left and right marked with yellow arrows.

Figure 4.14 gives an overview of the point of the short. The big light grey area in the middle is the big source field plate which overlaps the gate fingers. Also the antiparallel structure of the chip can be observed by the next gate to the right.

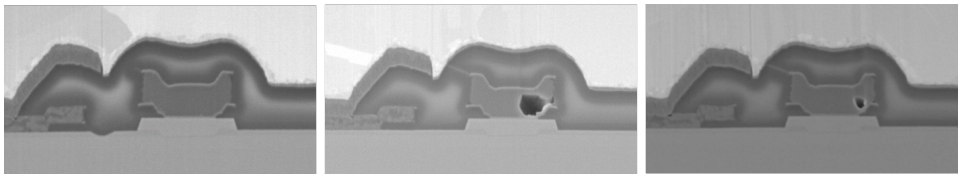


Figure 4.15: Series of three SEM pictures after FIB cuts along the gate finger axis (normal to the picture plane) showing the begining middle and end of the point of failure

In Figure 4.15 a series of SEM pictures, which were taken while milling through the damaged area via FIB, can be seen. In step two a hole where the gate aluminium is missing can be seen. Additionally a fine line connecting the gate finger with the source field plate can be seen on the upper right edge of the gate finger.

In the elemental map shown in Figure 4.16, the fine line can be identified as the missing aluminium. The short circuit of gate and drain is formed by the protruding

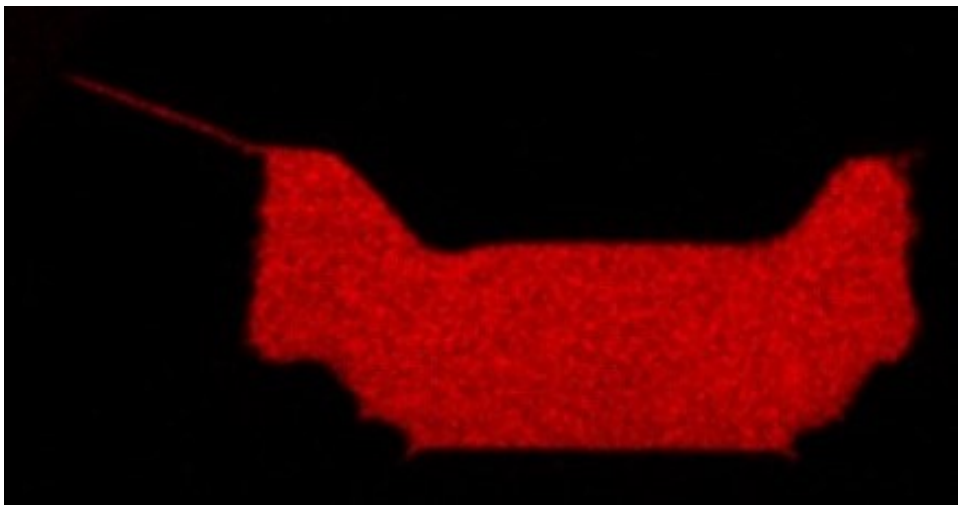


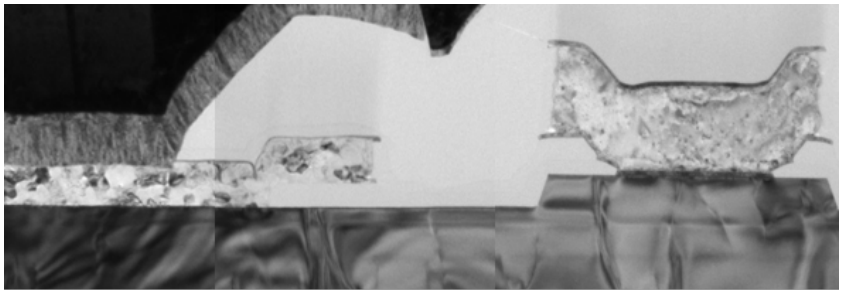
Figure 4.16: Elemental map at the point of protrusion. It can be clearly seen that the crack in the ILD is completely filled with aluminium from the gate finger causing an electric short between gate and source.

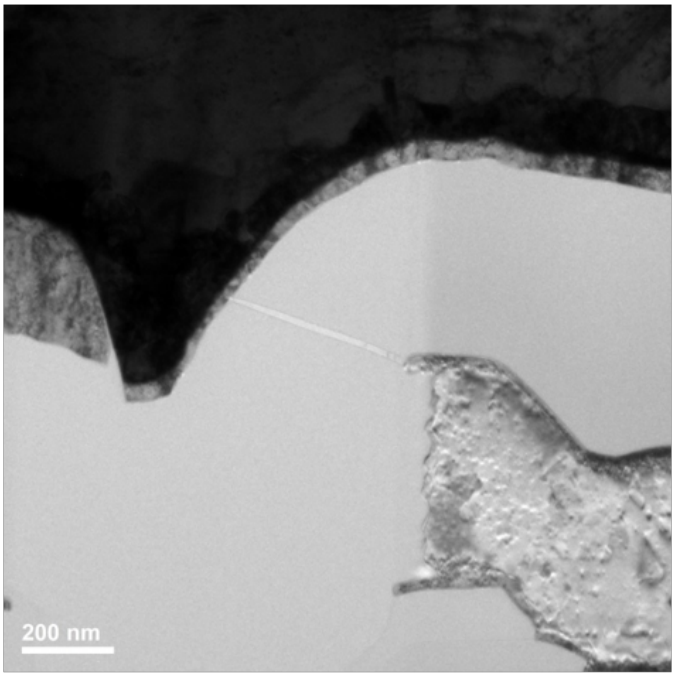
aluminium from the gate finger. Further magnification shows the exact spot of origin of the protrusion (Figure 4.17).

What can be seen in Figure 4.17 is that two different effects lead to the short circuit. First, the encapsulation of the gate finger is broken to form a crack from the gate finger to the source field plate. Second, this crack is filled with aluminium to get an electrical contact. The first hypothesis regarding the failure mechanism was that the aluminium melts up. This phase transition of first order gives a sudden increase of the volume, which could explain the failure picture. To confirm this hypothesis further physical failure analyses were conducted. For that reason a couple of chips were analyzed in depth, but these two features could never be found separately, which means that no crack was found, which was not filled with aluminium. This allows the conclusion that the aluminium protrudes its way through the ILD.

In case, the assumption of the molten up aluminium holds true, it must be possible to find physical evidences for the molten phase. To find them, a TEM lamella was prepared in the vicinity of the failure spot. From this lamella a bright field image was taken, which was compared with a reference image from a completely unstressed chip, see Figure 4.18.

It can be easily determined that the microstructure and the dislocation density equals in both of the pictures. This would not be the case if the failed gate aluminium had been molten up and recrystallized again. It can also be observed that the failed gate in its microstructure is homogeneous, which cannot be the case if the metal just partly melts up. A second set of pictures was taken by Scanning Transmission Electron Microscopy





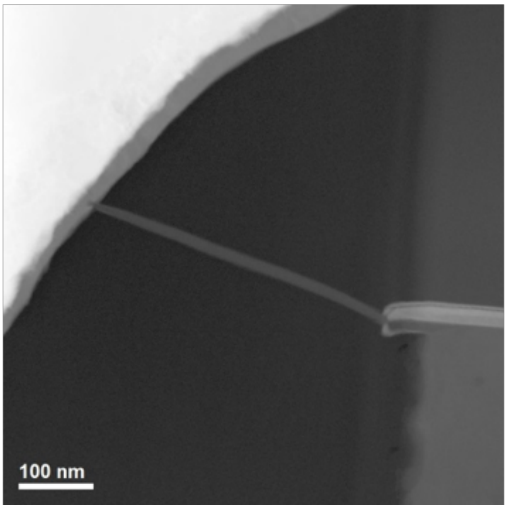


Figure 4.17: Overview and magnification of the protrusion in a TEM image.

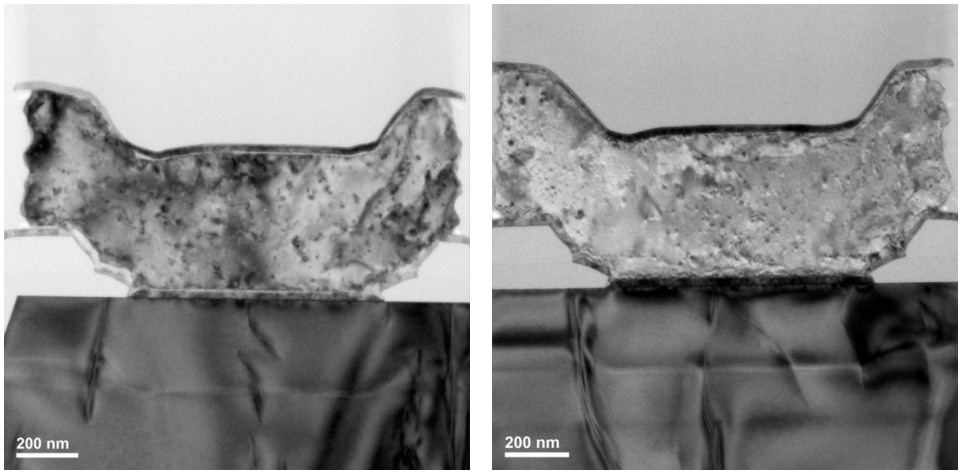


Figure 4.18: Bright field TEM images of reference (left) and with failed gate (right).

(STEM) and High-Angle Annular Dark-Field (HAADF), also on a failed and on an unstressed gate finger for comparison.

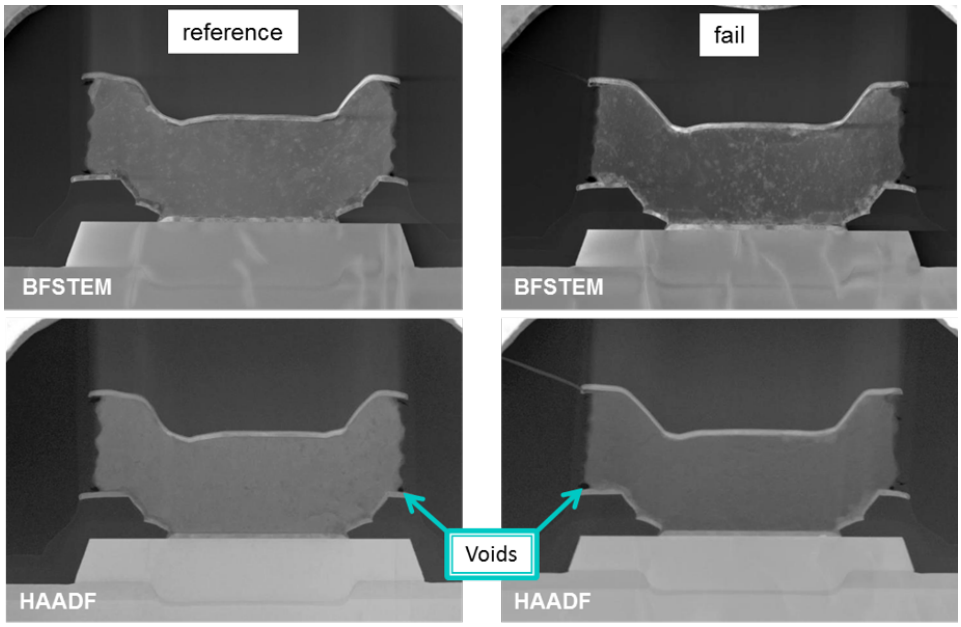


Figure 4.19: STEM and HAADF of gate area. The left picture shows a reference chip, whereas the right one shows a failed region.

Figure 4.19 shows on the left the gate metal sitting on top of the p-GaN. It can be observed that the gate metal is enveloped by a hard metal on top and on bottom, which can be seen by the brighter gray. Due to the structuring process of the gate metal, the covering layer on top is larger than the underlying aluminium layer. This is due to the etching process, which yields different etch rates on the covering layers and the

aluminium. After the structuring of the gate, the chip is covered in ILD. This sequence of processes leads to characteristic voids on the edges of the gate aluminium, which can be seen in the corners of the gate aluminium in Figure 4.19. The interesting observation is that these process induced voids are still present at the point of failure in the stressed chip. This proves beyond doubt that the aluminium of the gate is not molten up at the end of the short circuit pulse, otherwise these volumes would be filled.

These two evidences prove that the aluminium does not melt up during a short circuit pulse, which complicates explaining the failure. To overcome that issue, the simulation was expanded to a thermomechanical model taking a deeper look on the mechanical side of the problem.

4.5 Thermomechanical model

Since the pure thermal simulation of the short circuit pulse was not showing a melt up of the aluminium of the gate finger, which is in line with the physical failure analysis, a mechanical simulation was required. The target of the simulation was to take a closer look at the mechanical situation in the gate finger during a pulse. In this case it is not necessary to do a fully coupled thermomechanical simulation, since the mechanics cannot influence the thermal simulation as no cracks and/or big deformations are considered. Thus it is sufficient to calculate the mechanical field according to the thermal field at each time step of the simulation. For the mechanical simulation the mechanical parameters listed in Table 4.2 were used for the materials in place.

Table 4.2: Mechanical properties of all used materials. (most values are taken from [GT13], the rest are company internal measured values)

	Young's modulus E_{mech} G(N/m^2)	**Poisson ratio** ν (1)	**coefficient of thermal expansion** α_c m(1/K)
mold compound	32.4	0.21	6.1
imide	1	0.35	3.9
gold	70	0.44	14.2
aluminium	68	0.33	23.0
GaN	394	0.35	5.6
silicon	188	0.28	2.6
die attach	132	0.35	5
lead frame	120	0.34	16.5

As indicated in Table 4.2, only the gold and the aluminium feature plasticity. This is due to the fact that all the other materials are brittle and therefore would rather break than show plastic deformation. To model the plasticity in these two metals, a simple Bilinear Kinematic Hardening Plasticity (BKIN) model, which features rate-independent plasticity, was used.[1]

4.5.1 Mechanical boundary conditions

The mechanical boundary conditions were applied as follows.

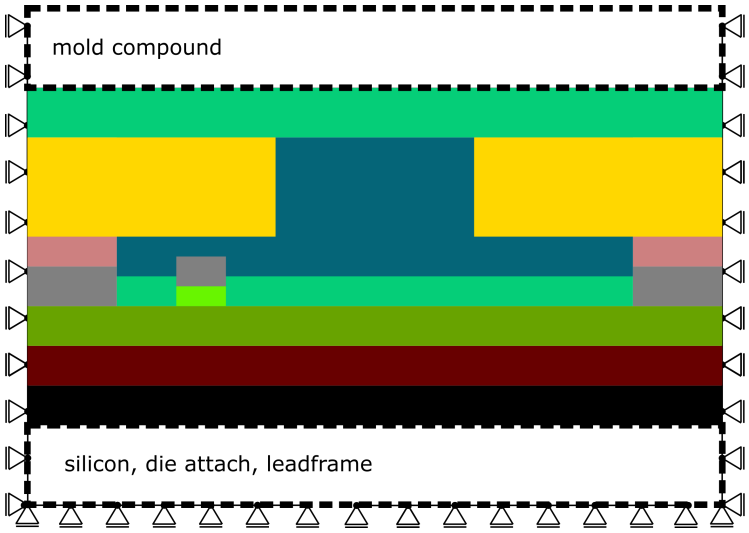


Figure 4.20: Mechanical boundary conditions of the single cell model.

As shown in Figure 4.20, the two nodes on the bottom left an right corner was completely fixed, i.e., in x and y direction, where the rest of the bottom nodes were only fixed in y direction enabling sliding of the bottom line. The nodes to the left and the right border of the model were fixed in x direction so that also a sliding along the y direction is possible.

This setup makes it possible that the single cell can expand in height but is confined to the left and right. This can be understood when we look at the simulation results within the time frame of the short circuit pulse. Normally, one would expect the chip to bow if it heats up. However, as the heating pulse is that short, the chip does not experience significant bending, which is reflected by the boundary conditions.

[1] In Table 4.2 just the elastic part of the material model is given.

4.5.2 Mechanical results

In the subsequent simulations first the thermal problem was solved and then for chosen times the mechanical problem was solved. Immediately it can be seen in Figure 4.21, that the highest stresses form at the edges of the gate finger in the covering ILD. To properly asses the value of those stresses a mesh refinement was introduced in the prone edges. Then a suitable area around the corner not including the deviated border elements was selected and the stress was quantitatively assessed there.

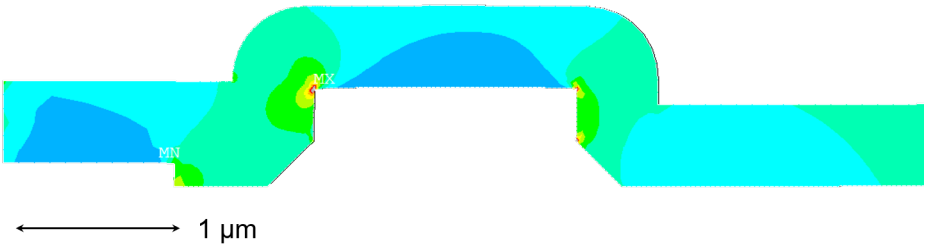


Figure 4.21: Overview of the stress in the ILD layer. It can be seen that the peak first principle stress areas are located on the gate edges. Compared to Figure 4.19 or Figure 4.18 that the geometry of the gate finger has been simplified without affecting the overall result.

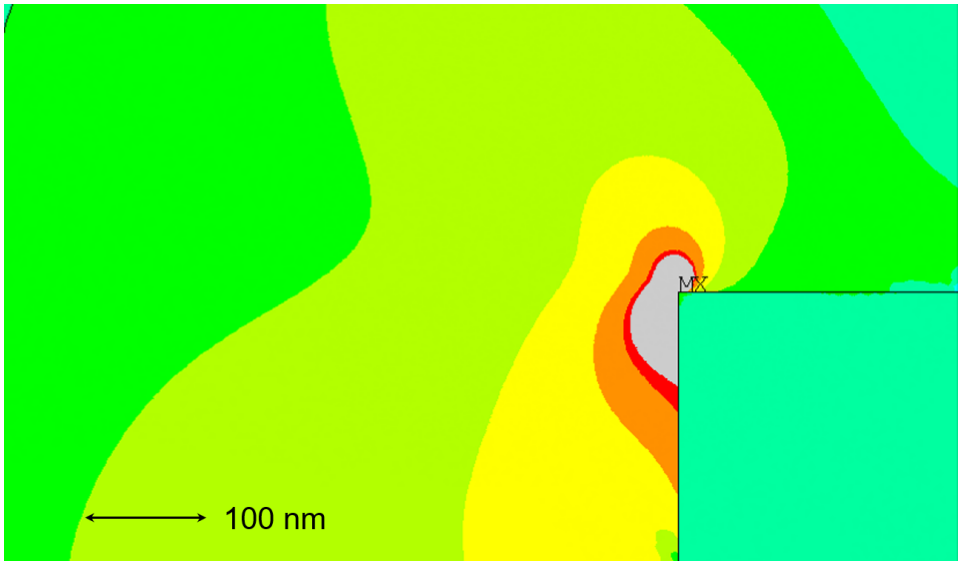


Figure 4.22: Magnification of stress on the gate edge facing the source side.

As can be observed in Figure 4.21, at the two corners where cracks in the ILD can be found, also the stress reaches maximum values. Deeper investigations revealed that the

stress concentration is higher on the gate edge facing the source side, which is in line with physical failure analysis. Physical failure analysis showed that cracks appear only on the edges of the gate facing the drain or the source side. Analyses of the stressed DUT show that the edge facing the source side are far more prone to failure. This is reflected in the simulation by the higher stress on the source side.

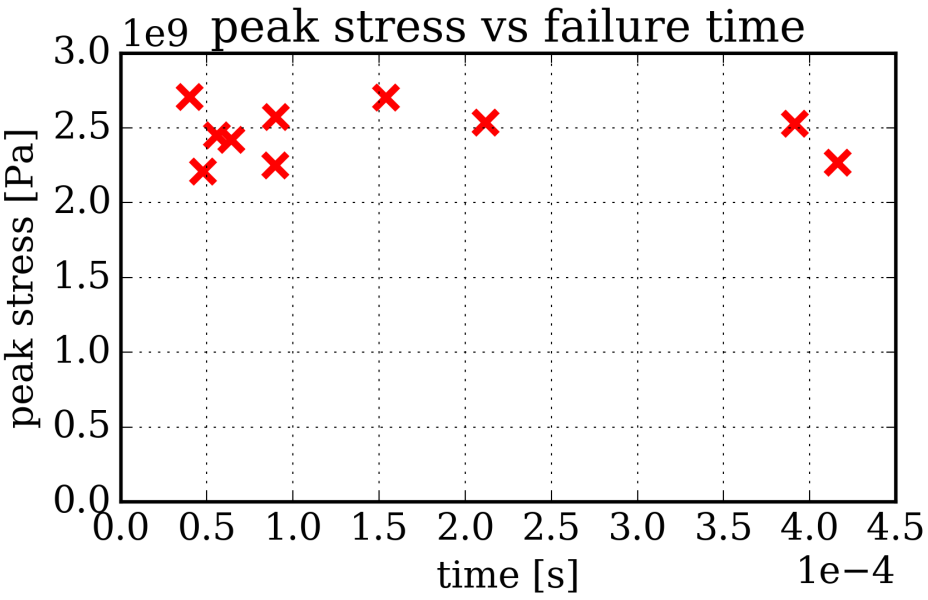


Figure 4.23: Maximal first principle stress of all pulses at the end of the short circuit pulse.

Simulations for all stressed chips show that the peak value of the first principle stress at the end of the short circuit pulse is very narrowly distributed. This gives a strong indication that the physical parameter, the first principle stress, is the root cause of the protrusion. The first principal stress values of all pulses is around 2.5 GPa (compare Figure 4.23), which is in the range of ultimate strengths reported for SiO_2 [Sha+15]. This simulation result confirms the physical failure analysis finding that the short circuit is formed by a protrusion. The direction of the crack seems to follow process seam lines, which pose prone crack directions since the material is weakened there.

4.6 Countermeasures

Since the root cause of the short circuit failure is confirmed by physical failure analysis and explained by simulation, a closer look at possible countermeasures needs to be taken. The high stress in the aluminium of the gate metal results from the high temperatures,

which cannot be avoided, in combination with the high Coefficients of Thermal Expansion (CTEs) of aluminium, which significantly differs from the CTE of the other materials. Without taking technological and or process considerations into account and just looking at the short circuit performance, different gate metals with a lower CTE would cause less stress an therefore improve the pure short circuit performance. Since changing materials in a chip design is a huge change, technology and process wise, other more subtle changes are investigated as well. From classical fracture mechanics [PF08] we know that edges always act as stress concentrators. In order to avoid this stress concentration, the classical approach is to round the corners.

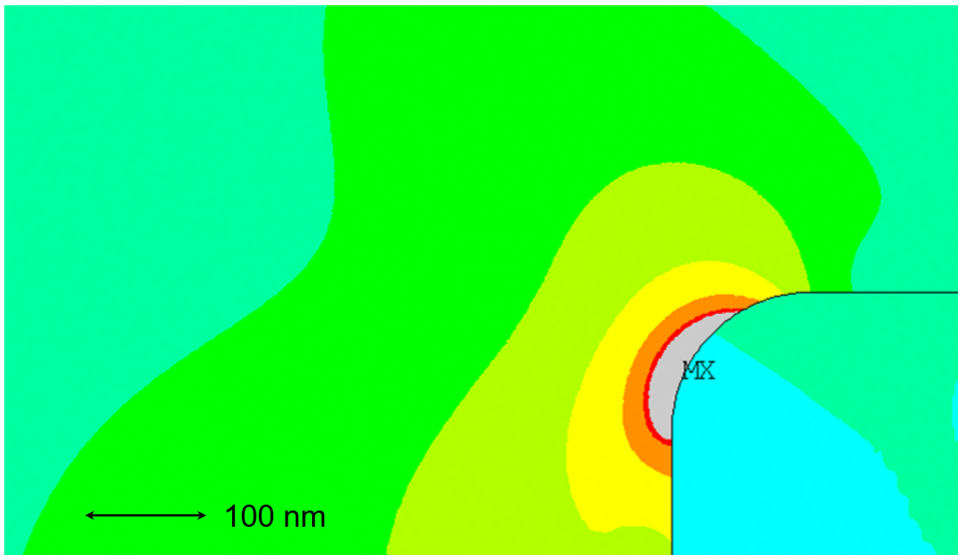


Figure 4.24: Magnification of stress on the gate edge facing the source side with a rounding of the edge.

The implementation of such roundings in our FEM model shows that the peak stress and also the surrounding stress field is reduced, which can be seen in Figure 4.24 featuring the same color mapping as Figure 4.22. To get an accurate picture of the situation in the prone corner also the overhanging, roof like, metal layer (see Figure 4.17) is further investigated. As can be also seen in Figure 4.19, the hard metal layer overtops the aluminium. This is a result of the structuring process of the gate finger, which was explained in Section 4.4. The roof shaped edge yields a significantly reduced stress in the FEM simulation. The resulting stress level is comparable to the stress of rounded corners with a radius of 30 µm. Since rounding edges pose significant process challenges, the roof structure with the hard metal layer is the ideal structure to avoid a sharp edge as stress concentrator and reduce the peak stress within the possibilities of semiconductor structuring processes. This means that no economically feasible changes can be made increasing the short circuit robustness.

4.7 Short circuit performance

This chapter showed how the massive thermal overload failure was provoked in a short circuit situation. The electric failure picture was described and physical failure analysis was conducted. The physical failure analysis in combination with FEM simulations showed that the failure can be explained by thermomechanical means. The root cause, a protrusion on the gate finger, caused by the high thermal gradients and different CTEs was identified. The actual situation in the chip was assessed, which show that the present geometric features provide a high sophistication against this failure mode.

Chapter 5

Piezoelectric resonances

In contrast to the previous chapter, where the temperature was the main force, in this chapter the reverse piezoelectric effect plays the main role. The reverse piezoelectric effect, as described in [Bir95], can be understood as a mechanical reaction to an applied voltage. This means that depending on the material and the applied voltage, the object reacts with contraction or expansion and or shear in one or multiple directions. The voltage can be applied in a harmonic way, which would excite the piezoelectric material also in a harmonic way. Basic mechanics calls this case forced vibration [Dem18]. Since every object featuring a stable equilibrium state is called a resonate system [KS13], it can swing and resonate. Every resonate system features eigenfrequencies also called natural frequencies. These natural frequencies can be used in technical applications like ultrasonic motors [Uch98], or can lead to catastrophic failures like the Tacoma Narrows Bridge disaster in 1940.

(a) Ultrasonic motor used in an auto focus objective in photography. [Ter08]

(b) The original Tacoma Narrows Bridge roadway collapsing. [Bot10]

Figure 5.1: Examples of resonance phenomena in daily life.

At this point note that the main findings are already published in an IEEE Transactions on Power Electronics article [Pri+20] and an article in the Microelectronics Reliability journal [Pri+18].

5.1 Circuit in resonance

Usually, Gallium Nitride (GaN) High Electron Mobility Transistors (HEMTs) are sold and used in a package. This is conventionally done by gluing or soldering the bare die on a lead frame and then molding it. The natural frequency of such an assembly can be roughly estimated, by simplifying the system to an Euler Bernoulli beam. Derived from the Lagrange equation of the beam following [Hab15], the governing equation can be written as

$$E_{mech} I \frac{\partial^4 \omega}{\partial x^4} = -\rho A \frac{\partial^2 \omega}{\partial t^2} \tag{5.1}$$

with E_{mech} as the Young's modulus, I the second moment of area and A the cross section of the beam. Following [Mau09], the spatial part of Equation (5.1) can be solved by

$$\omega^2 = E_{mech} I \cdot \frac{1}{\rho A} k_x^4 \tag{5.2}$$

with transcendental boundary condition for the wave number k_x

$$\cosh k_x l \cos k_x l = 1 \tag{5.3}$$

Since the biggest and stiffest part in such a chip assembly is the lead frame, it is the dominating part. Typical lead frame dimensions (lxbxh) are 20 mm x 10 mm x 1 mm, made out of Copper (Cu) with a Young's modulus (E_{mech}) of 117 GPa [LZ12] and density (ρ) of 8960 kg/m^3. Equation (5.1) combined with the first numerical solution of Equation (5.2) yields the first natural frequency:

$$f = k_{x_1}^2 \sqrt{\frac{E_{mech} I}{\rho A}} \frac{1}{l^2} = \frac{4,73\ldots^2}{2\pi} \sqrt{\frac{E_{mech} \cdot \frac{bh^3}{12}}{\rho b h}} \frac{1}{l^2} \approx 10\,\text{kHz}. \tag{5.4}$$

Since GaN HEMTs typically operate with switching frequencies ranging from 10 kHz to 1000 kHz, the natural frequencies of our chip assembly are of major importance. During the switching operation a cyclic voltage is applied to the HEMT. Due to the fact that the source is normally connected to the backside of the chip, the GaN layer experiences

a lateral and a vertical field, which in combination with the piezoelectric tensor of GaN [NOH12] orientation in the device

$$\begin{bmatrix} S_1 \\ S_2 \\ S_3 \\ S_4 \\ S_5 \\ S_6 \end{bmatrix} = \dots \begin{bmatrix} 0 & 0 & d_{31} \\ 0 & 0 & d_{31} \\ 0 & 0 & d_{33} \\ 0 & d_{15} & 0 \\ d_{15} & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} E_1 \\ E_2 \\ E_3 \end{bmatrix}, \tag{5.5}$$

causes a displacement in all three directions of the chip. Here the GaN layer acts as an actuator on the whole chip assembly.

Due to the fact that Equation (5.4) has shown that the natural frequencies lie within the applicative frequency range, the scope of this chapter is to assess the reliability implications of this resonate assembly. The focus hereby lies on the stresses in the GaN layer and the solder, since these are the most prone components under mechanical loading. Usually mechanical stress is derived from mechanical strain, which can in principle be measured. However, since the assembly as a whole and the components to investigate are very small, many measuring techniques cannot be applied. What further complicates the problem is the fact that the stress is only present when the assembly is in resonance and therefore moving very fast. This cancels contact less techniques like X-ray and neutron scattering out, for which reason a different indirect approach had to be used. Therefore, a Finite Element Method (FEM) model of the assembly was built to get insights into the resonant stresses via the model. For calibration the much easier to measure deflection shapes and displacements on the outside of the package were used.

5.2 Measurements

To measure the resonance effects, the chip must be exited in the right way, which means applying a sufficient sinusoidal voltage. Due to the nature of the reverse piezoelectric effect, it is enough to apply an electric field to the piezoelectric layer, with no substantial current. The easiest way to achieve a forced vibration is to apply a sinusoidal voltage to the chip.

The measurement was done by using a Laser Scanning Doppler Vibrometer (LSDV), explained in detail in Section 2.2.2. In short, as its name suggests, the LSDV utilizes the Doppler-effect to measure velocities on reflecting surfaces.

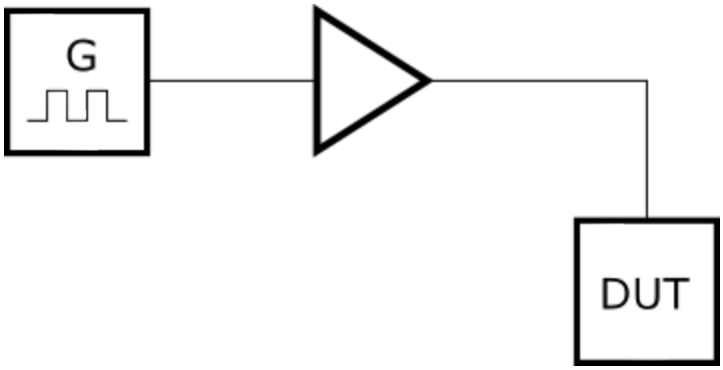


Figure 5.2: Principal circuit diagram of the excited DUT.

The function generator, highlighted by G in Figure 5.2, is connected to a high voltage amplifier to reach the voltage levels that are present during applicative use. This high voltage signal is then directly applied to the DUT. The voltage used was 200 V. This high level of voltage implies that security measures have to be applied to protect the whole assembly against accidental contact. Therefore, the complete assembly was placed in a specially constructed housing.

The protective housing can be completely removed from the base plate to give unhindered access to build up the assembly. After the initial build up, the hood can be turned over the assembly. For minor changes the front door can be opened. The front door as well as the hood itself are locked if the sensing element of the protective housing measures more than 50 V. The swinging DUT can still be measured with the LSDV through the adjustable holes on three sides of the box.

Further, the protective housing box including the assembly is mounted on an optical table to isolate it from the swinging of the building.

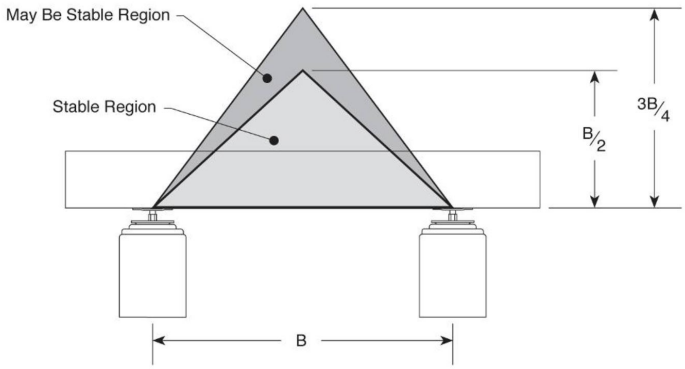


Figure 5.3: Pyramid of stability of the passively damped optical table. [14]

The optical table has a rigid top plate, making it impossible to have a relative motion between the measuring head and the swinging DUT. The rigid top plate and the damping system reduce the natural swing of the building visible in the low frequency regime of the measurement. The stability regions are highlighted in Figure 5.3.

With this setup, several measurements were taken. In a first step a simple endurance test was performed in a preliminary fixation. For this test, the chip was mounted and a natural frequency spectrum was taken. Then the resonance frequency with the highest displacement was animated with a sinusoidal signal for an elongated period of time (approximately one week). Afterwards the resonance frequency spectrum was measured again. Comparing the resonance spectral before and after the long high resonance test, gave an exact match. The reason for this preliminary test was to check for failure, which would result in a change of the frequency spectra, as failure causes internal structural changes of the chip e.g. by cracks.

These preliminary measurements uncovered two important topics. The clamping is very important. With the simple clamping mechanism of the burn in socket, it is impossible to reproduce a measurement nor is it possible to get the the exact clamping point and force for the follow up simulation. Secondly, the resonance is not causing serious damage within the chip, so the device can be safely used for further measurements. To this end, we will investigate a high cycle fatigue phenomenon to determine how far away from the point of catastrophic failure the resonance is.

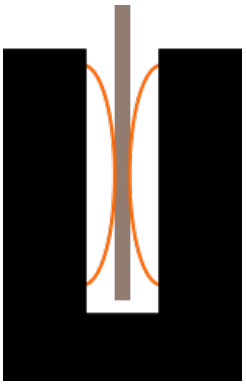
5.2.1 Clamping mechanism

At the beginning a simple burn in socket to just electrically contact the DUT was used.

As can be seen in Figure 5.4, the socket is ideal to easily electrically contact and mount a chip. The problem lies in the mechanical boundary conditions, required for the FEM simulation. To be more precise, with this type of mount neither the location nor the force acting on the legs of the chip can be exactly determined. Thus, this type of fixation is not suitable to be reproduced in a FEM model. To overcome this issue, an investigation about the proper fixation was conducted. The main aim of the clamping mechanism is to give defined mechanical boundary condition. To achieve locally defined boundary conditions a mini bench vise was constructed. This mini vise clamps the legs from both sides as can be seen in Figure 5.5.

Since the legs of the package are in contact with the jaws of the vise, they need to be electrically isolating. A simulation was conducted to determine to what extent the legs should overlook the jaws. This is indicated by the green area in Figure 5.6.

(a) TO-220 burn in socket. [DHg19]



(b) Clamping principle of the socket.

Figure 5.4: TO-220 socket used to establish electric contact.

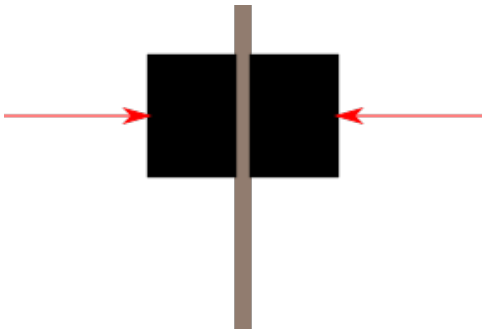


Figure 5.5: Adapted clamping, where the legs of the package are pressed by the jaws of the vise, giving defined mechanical boundary conditions.

Two extreme cases could be identified. On one the hand, if the free leg length is reduced to zero, the rest of the housing blocks the chip from swinging. On the other hand, the if the free leg length is very long, the main displacement is found in the flexible legs and not in the chip itself. A parametric study showed that most pronounced swinging will take place in the chip if the free leg length is reduced to a minimum around 1 mm to 2 mm.

The final decision of the free leg length was taken to 1 mm. To get this distance in a reproducible way a small metal plate with the thickness of 1 mm was used. This plate was inserted during mounting between the jaws of the vise and the package and was removed before measuring. This resulted in a defined a reproducible free leg length.

With this new mount, two types of measurements were conducted, spectral measurements and scanning measurements explained in the next sections.

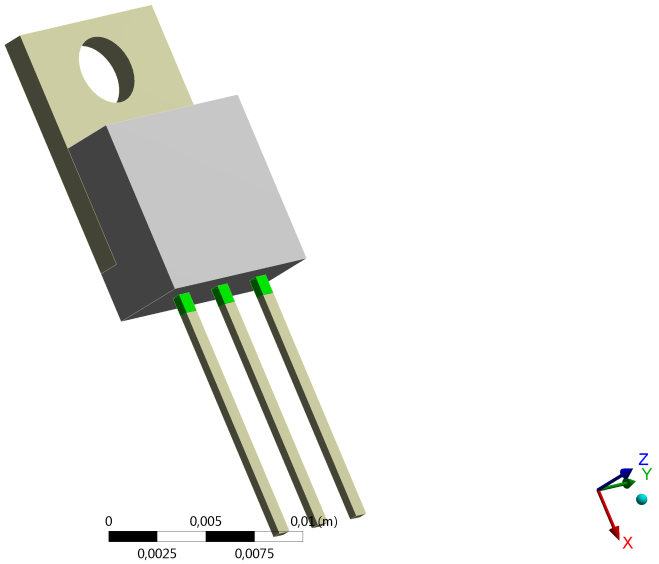
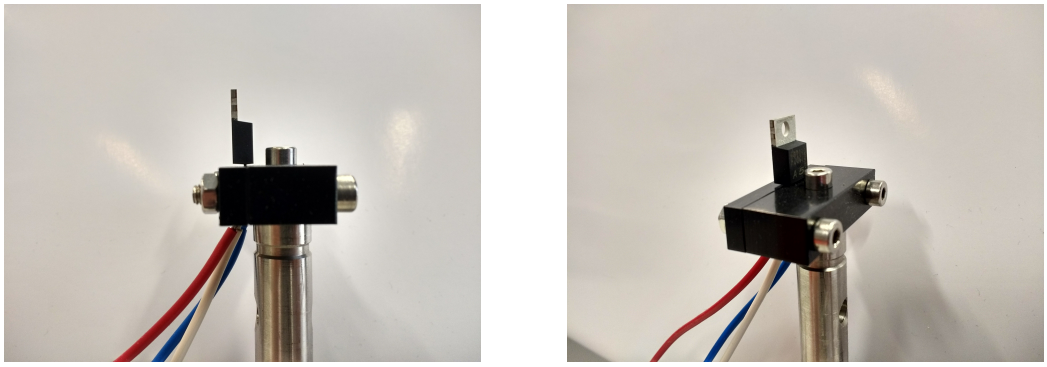


Figure 5.6: Model of a TO-220 package. The signal green part of the legs is free while the other part is fully clamped. The length of the green part has been varied to find the optimal free leg length.



(a) Side view on the DUT in the new camping vise.

(b) Isometric view on the DUT in the new camping vise.

Figure 5.7: New clamping mechanism with the DUT mounted.

5.2.2 Spectral measurements

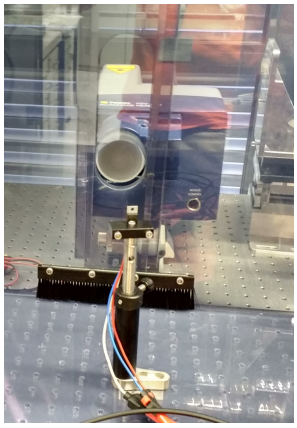
Spectral measurements show the response of a structure to an excitation in a frequency range. For this measurement a frequency sweep was applied to the chip using the output of the synchronized function generator of the PSV-400. Since the Digital-to-Analog Converter (DAC) in the function generator produces a signal with visible digitization steps, a smoothing capacitor board was soldered to the output.

The measuring procedure was the following:

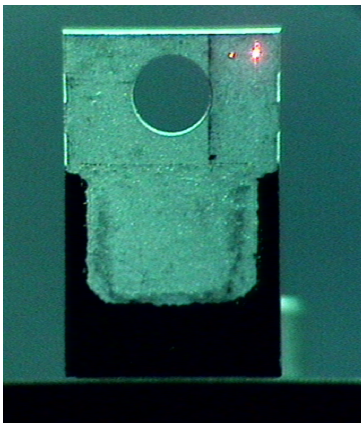
- The package was mounted in the vise, in such a way that the backside of the package was normally oriented to the optical axis of the LSDV.
- Then the distance from the scanning head was adjusted such, that with a middle zoom level the full package filled the optical sensor of the LSDV, making it easy to focus.
- By the help of the zoom, a fine adjustment, to get the full package backside as big as possible, is done.
- With the optical auto focus a sharp picture was achieved.
- Then the laser auto focus was adjusted to get the smallest possible scanning point on the measured surface. (After completing the steps above in the LSDV Figure 5.8b can be seen.)
- The scanning plane is defined in the LSDV software by the corner points of the package and a few scattered points (chosen by the software) in between.
- Then the scanning area was defined to the visible back side of the package, sparing out the mounting hole of the lead frame.
- The scanning points were placed on the scanning area using a regular grid.
- Lastly, step all defined scanning points were calibrated automatically by the software.

For excitation a frequency sweep from 2000 Hz to 200 000 Hz was applied. Several points on the backside of the chip need to be measured. This is necessary due to the fact that all swinging shapes feature points where no deflection is observed. These points are called swinging knots. If a sweep measurement is taken in one of these swinging knots, no deflection (and therefore resonance) can be seen at this frequency. To avoid missing resonances several points marked by red circles in Figure 5.9 have been measured.

Figure 5.10 shows the raw measured results from the frequency sweep. It can be observed that none of the measuring points is situated in a swinging knot. Furthermore, it can be seen that the two upper points and the two lower points show qualitatively and quantitatively the same behavior. Such a behavior can be observed if the chip and the eigenshape features a symmetry axis between left and right with respect to Figure 5.8b. This information will be included later in the simulation. For all further investigations the upper left curve will be considered, since it shows the highest displacements.



(a) DUT placed in HV housing. In the background the scanning head can be seen.



(b) View through the LSDV on the DUT.

Figure 5.8: Measuring setup and view of the DUT through the LSDV.

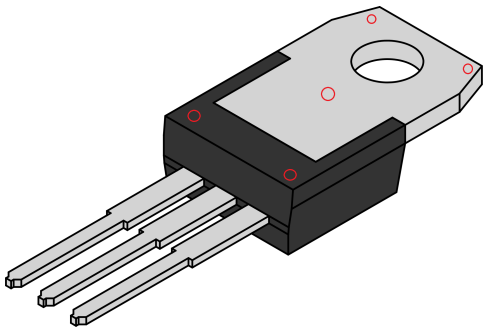


Figure 5.9: T0-220 backside view [Ind07].
The final measuring points for the spectral are marked in red.

Due to the mechanical decoupling from the laboratory environment, the low frequency spectrum shows a relatively low noise level and even smaller displacement resonances (below 25 kHz) can be seen. The fit of the seven biggest resonances in Figure 5.11 also shows the quality factor Q_{mech} of each of these resonances. For the fit itself Equation (5.6), the solution of a driven harmonic oscillators, called Lorentz curve [Hab15] was used

$$u(f) = \frac{A_0}{\sqrt{[(2\pi f)^2 - (2\pi f_0)^2]^2 + (2\gamma \cdot 2\pi f_0)^2}} \tag{5.6}$$

With this shape of resonance, the quality factor is defined as follows:

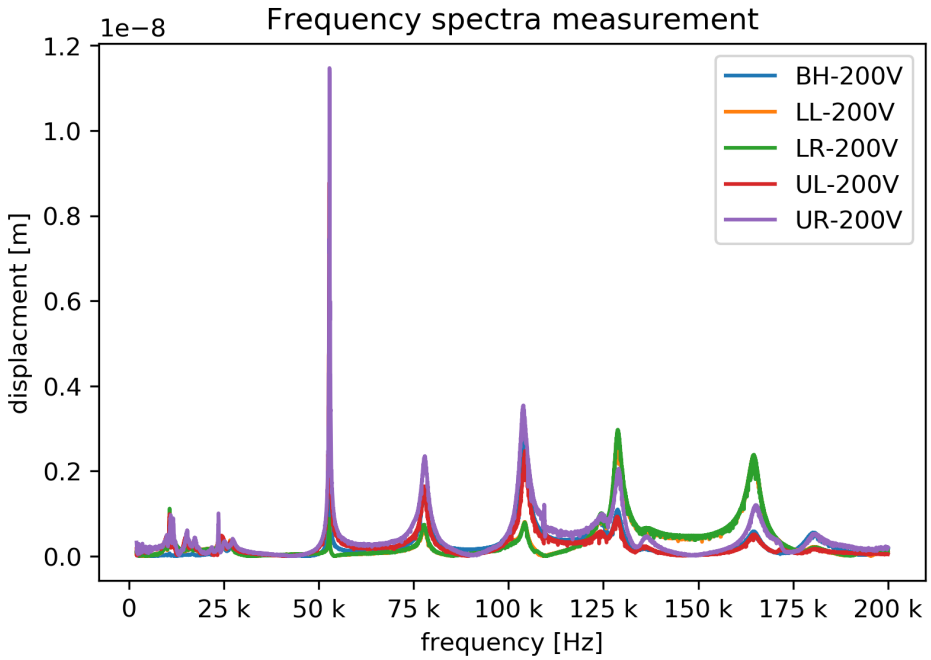


Figure 5.10: Frequency spectra of the five points marked in Figure 5.9. (LL = lower left, LR = lower right, UL = upper left, UR = upper right and BH = body middle) showing seven clear and pronounced resonances (peak voltage used 200 V).

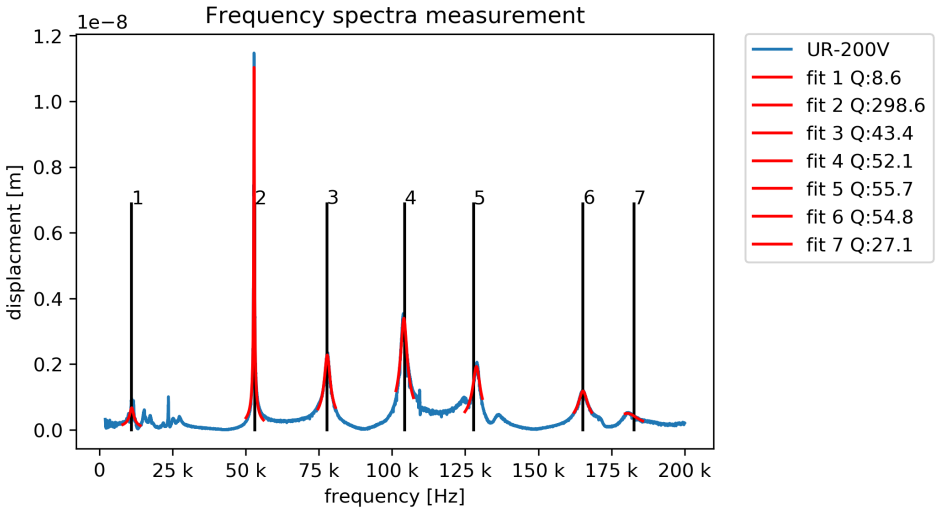


Figure 5.11: Analysis of the displacement spectral for the upper left reference point. All resonance peaks are fitted.

$$Q_{mech} = \left| \frac{2\pi f_0}{2\gamma} \right| \quad [1] \tag{5.7}$$

The quality factor is a dimensionless parameter characterising the damping of a resonance. The higher the value, the smaller the damping. In more illustrative physical sense the value can be interpreted (for bigger values) as the number of oscillations the free swinging system needs to undergo till the the resonance fades to $e^{-\pi}$ of its original amplitude.

What immediately sticks out in Figure 5.11 is the resonance number two slightly above 50 kHz with its high Q-value of nearly 300 . According to the high Q-value also the amplitude of this resonance is significantly higher than the others with a maximum displacement of 11.2 nm.

The main information extracted from the spectrum measurement is the frequency of the resonances, which we want to excite in the second step, the scanning measurements.

5.2.3 Spatial scanning measurement

In contrast to the spectral measurement, where the full spectrum of resonances was excited in the spatial scanning measurements just one single frequency was used. Combining these two measurements, in a scanning sweep, is in principle possible, but the results are very noisy eigenmode shapes which subsequently make them unusable in the further process.

Table 5.1 shows all identified resonances, including side maxima, which were explicitly measured across a grid of measurement points. For each measurement all grid points on the backside were measured sequentially with the LSDV. The software takes care if certain measurements fail, to repeat them, which results in a complete measurement of the backside of the chip.

The result can be seen in Figure 5.12 showing at each measurement point the normal[2] displacement. The colors in between are a linear interpolation between the measurement

[1] Note that from Equation (5.6) $\gamma \in \mathbb{R}$. If the function is defined this way Q must be defined with $||$, because the displacement is always $\in \mathbb{R}_+$. The absolute value function can be dropped if $\gamma \in \mathbb{R}_+$.

[2] This is the reason why it is so important to place the backside of the chip normal to the optical axis of the LSDV. Otherwise just the normal component of the displacement would be measured.

Table 5.1: Identified resonances from the spectral measurement with corresponding mode number and frequency.Note that also the side maxima are listed here

eigenmode number	frequency
1	9813 Hz
2	10 719 Hz
3	11 500 Hz
4	15 000 Hz
5	16 813 Hz
6	24 469 Hz
7	26 781 Hz
8	52 781 Hz
9	77 781 Hz
10	104 344 Hz
11	109 438 Hz
12	124 375 Hz
13	128 844 Hz
14	136 031 Hz
15	164 688 Hz
16	180 344 Hz
17	195 563 Hz

points. The points missing for a regular grid could not be measured by the software. Following the basic understanding of resonances it can be seen that the higher the mode number and the frequency gets, the more swinging knots can be seen (compare Figure 5.13).

With these two types of measurements, the resonance behavior of the test package can be fully described. From the spectrum measurement the frequencies of the resonances can be found, including their displacements at the measuring points. The scanning measurement yields the form of the resonance and again the maximum displacement which is consistent with the peaks found in the spectral measurement.

5.3 Chip design

In this section the explanation why in contrast to Chapter 4, a TO-220 with a simplified chip design is used, is given. First preliminary tests including the proof of the basic principle, of bringing the chip in resonance by applying voltage, were undertaken with a fully functioning HEMT package in DSO-20 mounted on a printed circuit board

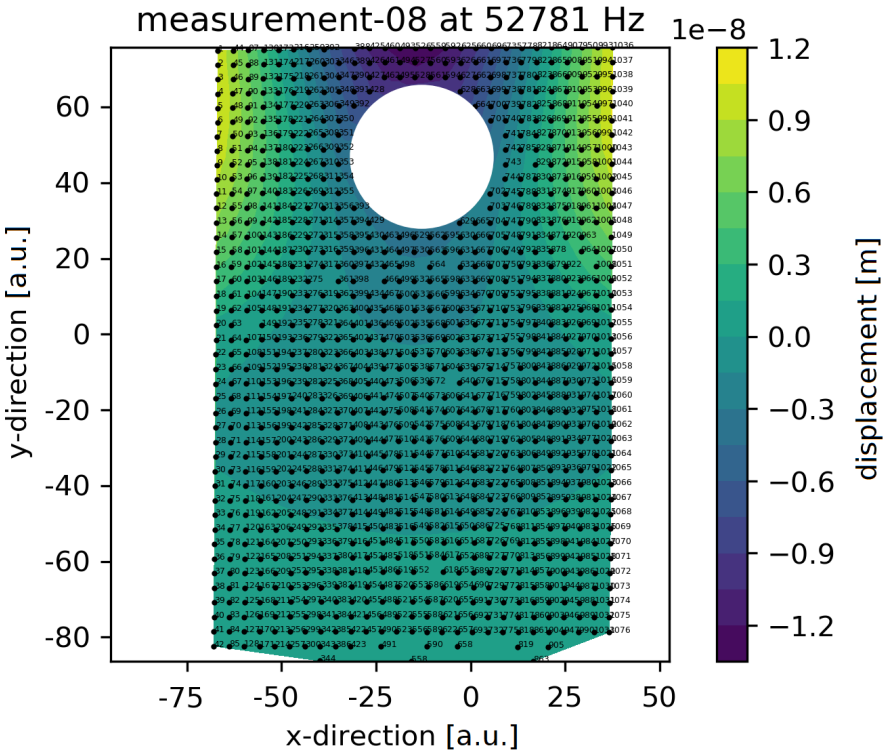
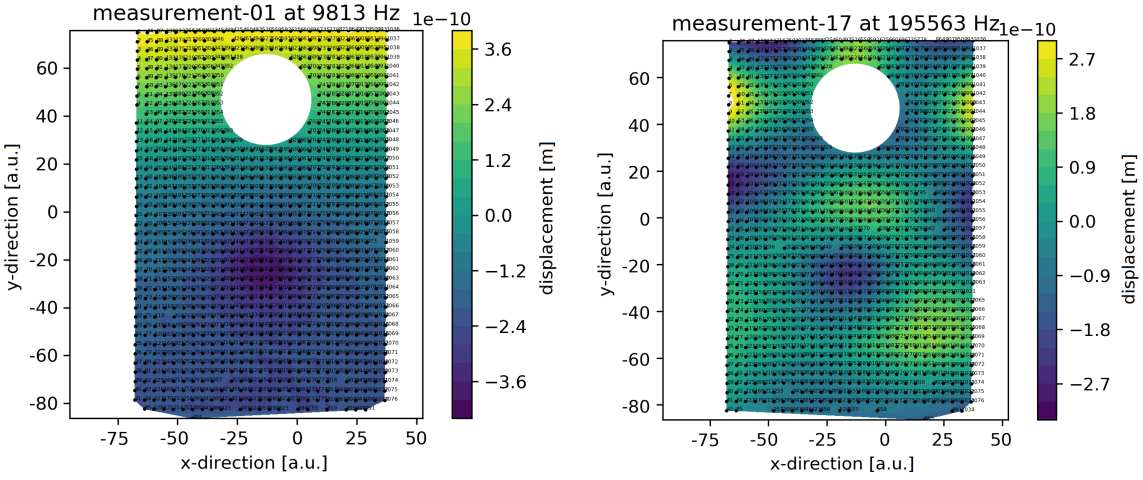


Figure 5.12: Scanning measurement of the resonance at 52 781 Hz.



(a) Measurement of the eigenmode 1 at 9813 Hz. (b) Measurement of the eigenmode 17 at 195 563 Hz.

Figure 5.13: Measurements of the highest an lowest eigenmode.

(PCB). This realization poses two main difficulties. As can be seen in the cross sections Figure 4.17, one unit cell measures in the range of µm. Since the unit cells are also placed in antiparallel and parallel sequences the electric field features relatively small structures compared to the overall size of the chip. The overall size of the model is determined by the package size including the PCB. This cannot be reduced, since the whole structure undergoes resonance and therefore must be simulated completely. To get an acceptable resolution of the electric field, the mesh size used would be so small that the whole model would feature an unsolvable amount of degrees of freedom. To overcome this problem, not a fully functional HEMT was used as a DUT, but a specially fabricated test chip. This test chip featured several characteristics compared to the chip used in Chapter 4.

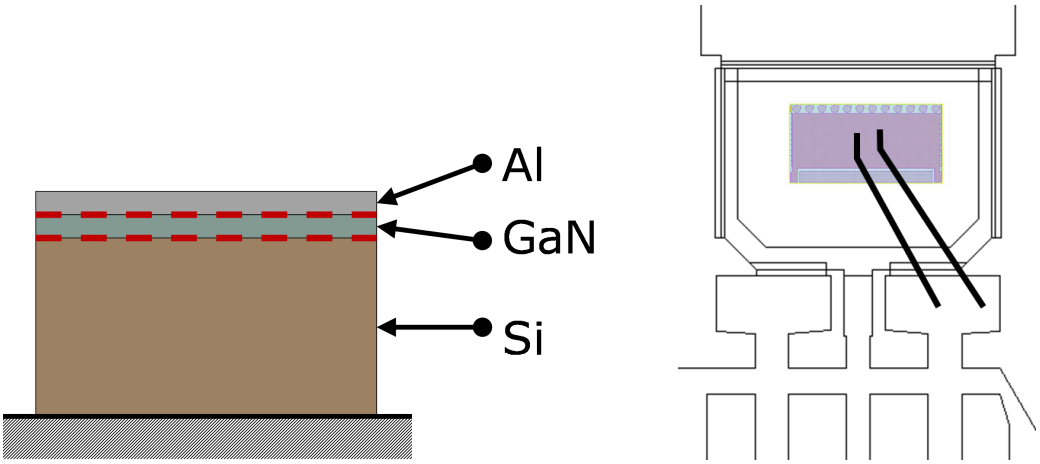
- The package was changed from a DSO-20 to a TO-220, which normally would not be optimally suitable for a GaN HEMT. This change also makes it possible to mount the chip with its legs without soldering it on a PCB.

- The internal structure features the stack of a GaN HEMT, but on the stack itself no HEMT structure (i.e. source, gate, drain) was processed. Instead a full metallization on top was deposited.

- Contrary to the HEMT featuring spatially small horizontal and vertical fields, the test chip just features a vertical electric field.

The vertical electric field is applied to the complete GaN stack, as can be seen in Figure 5.14a.

The silicon substrate is highly doped and acts as one electrode of the plate capacitor, while the top metallization acts as the other electrode. At this point note that basic electrostatic [Dem17] gives in a good approximation a homogeneous electric field between these two planar parallel plates. The substrate is soldered to the lead frame and is in electric contact with one leg, while the top metallization is bonded to another leg, as can be seen in Figure 5.14b. The layer marked with GaN in Figure 5.14a is in reality the sum of the adaption layers, the GaN buffer and the top Aluminium Gallium Nitride (AlGaN) layer. This simplified model results in an increased smallest feature sizes. One methodology used here is to homogenize this stack upfront so it can be treated as one homogeneous layer with equivalent characteristics and thus in bigger element sizes for the FEM simulation, which significantly reduced Degrees of Freedom (DoFs) of the model, making it possible to solve in a reasonable time.



(a) Schematic of the fabricated test structure. On a Silicon substrate a GaN layer is grown. The top layer is metalized with aluminium for a top electrode. The whole structure is soldered on a copper lead frame. The red lines symbolize the equipotential lines of the "parallel-plate capacitor".

(b) Bonding diagram of the chip.

Figure 5.14: Schematics of the test chip.

5.4 Model

This section describes the general construction of the FEM model. In principle all FEM models need to find a compromise between two fundamental contradicting characteristics:

- Accuracy and resolution of the model. These properties can be improved by increasing either the number of elements or the order of the elements, where the order of an element increases the order of the basis function (number of nodes along an edge of a 3-D element). Thus, both approaches increase the number of DoFs.

- Time to solve the model. To establish a reasonable work flow, the model needs to be solvable with the available computational power within a few hours. An absolutely correct model solved in years is of no use to anyone.

Standard procedures to reduce the computational cost are reducing the dimensionality of the problem, but cannot be applied in this setting, since the real 3-D structure has no direction of pronounced elongation, which would permit the use of plane stress or strain assumptions. Also the approach using a symmetry axis to half or even quarter the volume of the model cannot be implemented, since an exactly symmetric model can

just feature symmetry solutions, which were already falsified by the measurements, see therefore Figure 5.13b, where it can easily be observed that the bottom left and right side show different shapes and absolute deflections.

Preliminary trials with brute force meshing showed that meshing with hexahedral elements results in a tremendous amount of DoFs. So, the extent of the model and the smallest feature size make it necessary to manually mesh the model in an intelligent way.

In general, meshing is done from the smallest feature outwards. The smallest feature in our model is the GaN layer with a thickness of 3 µm. Starting from this length, divided by the necessary divisions (3 in this case), the smallest edge length is determined. From the ANSYS manual [Koh19] it is known that the:'...aspect ratio alone has little correlation with analysis accuracy.' Therefore, the maximum aspect ratio was set to the warning limit of ANSYS, which is 20 , creating plate like cuboids. First the GaN layer was meshed with the plate like cubes followed by all the bodies on the top and bottom. Then, from the middle block that is already meshed, the model is meshed outwards, starting at the height of the GaN layer. Afterwards, the corners and then the remaining unmeshed volumes are meshed.(For visual comparison, the meshing procedure is illustrated in Figure 5.15)

All these meshing steps are done in such a way as to avoid skewed elements and to keep the aspect ratio below the limit of 20 . Furthermore, the element size is chosen such that the elements get bigger the further away from the GaN layer, which contains the smallest features.

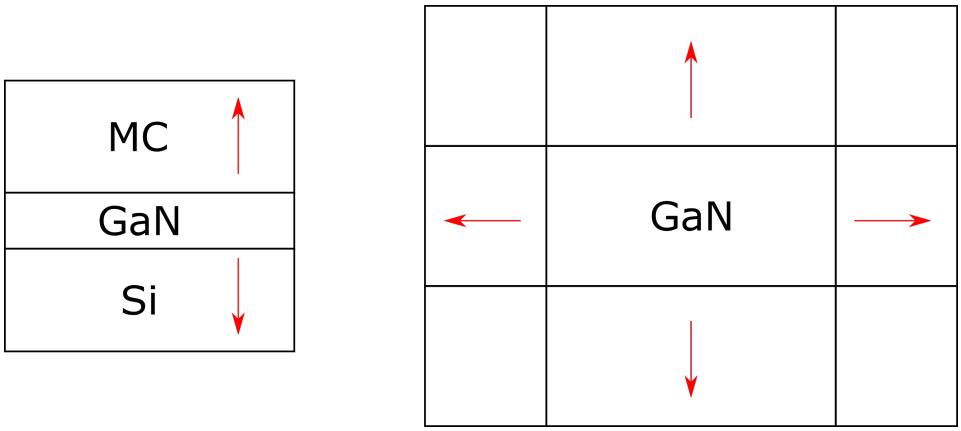


Figure 5.15: Meshing strategy for the test chip. The left figure shows the stack from a side view the right one a top view picture.

After meshing the model, a mesh convergence [ZTZ13] study had to be undertaken. Mesh convergence ensures that the result of the FEM model is accurate. FEM models, generally speaking, need enough DoFs to reproduce the quantitative shape in reality.

Take for an example a simple one sided fixed beam featuring a deflection shape [Ric08] of the form:

$$u(x) = \frac{F}{6E_{mech}I}(3lx^2 - x^3). \tag{5.8}$$

This shape cannot be captured by a few linear elements, because they can not reproduce the bending shape of the beam. Generally, in a mesh convergence study the number of DoF is increased and the response of a well chosen representative simulated value is observed, see Figure 5.16.

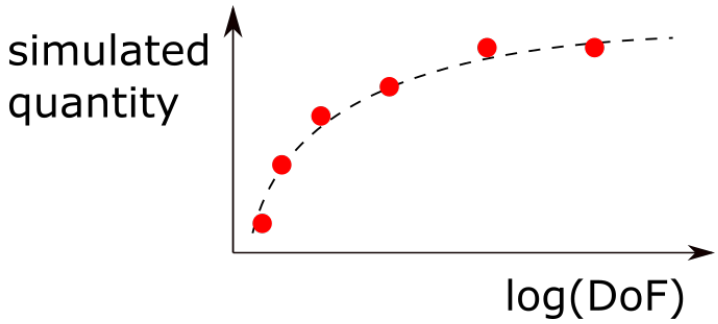


Figure 5.16: (Mesh) convergence of FEM models.

The increase of DoF can be done in two ways, by increasing the order of the basis function of the elements (in literature referred to as p-refinement) or by increasing the number of elements (in literature refereed to as h-refinement). Since in ANSYS the order of mechanical elements is limited by two (which were consequently used) an h-convergence study was conducted. The representative mechanical value used is the frequency of the first eigenmodes. How this value was obtained will be shown in the next section.

Table 5.2 shows the frequencies of the first ten eigenfrequencies of four different models. The worse model has a reduced number of elements while the refined models, refine 1 and refine 2, feature extensively more elements and therefore DoFs.

The mesh convergence study should help to distinguish and identify two extreme cases:

- Too small number of DoFs: As stated earlier this results in wrong results, as highlighted in Figure 5.16.
- Too to many DoFs: This setting results in saturated (correct) results, as shown in Figure 5.16, but consumes an inappropriate amount of time to solve.

Table 5.2: h-convergence study with the first eigenmode frequencies

	used model	**worse**	**refine 1**	**refine 2**
number of piezo electric elements	2960	2960	2960	5243
number of normal elements	286747	195360	255834	811609
mode number	freq (Hz)	freq (Hz)	freq (Hz)	freq (Hz)
1	794	816	798	792
2	7855	7895	7821	7832
3	13306	13653	12986	13253
4	18229	18291	18201	18201
5	26187	26283	26369	26155
6	27243	27381	27826	27156
7	33183	33456	34819	33042
8	40577	41799	42138	40439
9	58010	58048	58072	57984
10	62832	62916	64472	62795

The aim is to find the minimum number of elements, which ensure correct results, or to be more precise the needed accuracy. For the frequency of the first eigenmodes exactly the needed behavior is shown in Table 5.2. Even increasing the number of elements extensively results just in minor changes within the numerical accuracy. Reducing the number of elements results in a significant change, so the 'normal' model can be considered a good choice with regards to DoF.

Since the result should also capture asymmetric eigenmodes, the chip was placed non centered on the lead frame to get an asymmetric model.

5.5 Modal simulations

The first type of simulation conducted was a modal analysis. This type of simulation can be considered the be the simplified counterpart of the spectral measurements. A modal analysis gives the solution to the linear eigenvalue problem given in [Koh19][ZTZ13]. The eigenvalues of the linear system represent the resonance frequencies of the undamped system. Conveniently with eigenvalues also the eigenvectors can be calculated, which represent the deformation shapes of the resonance.

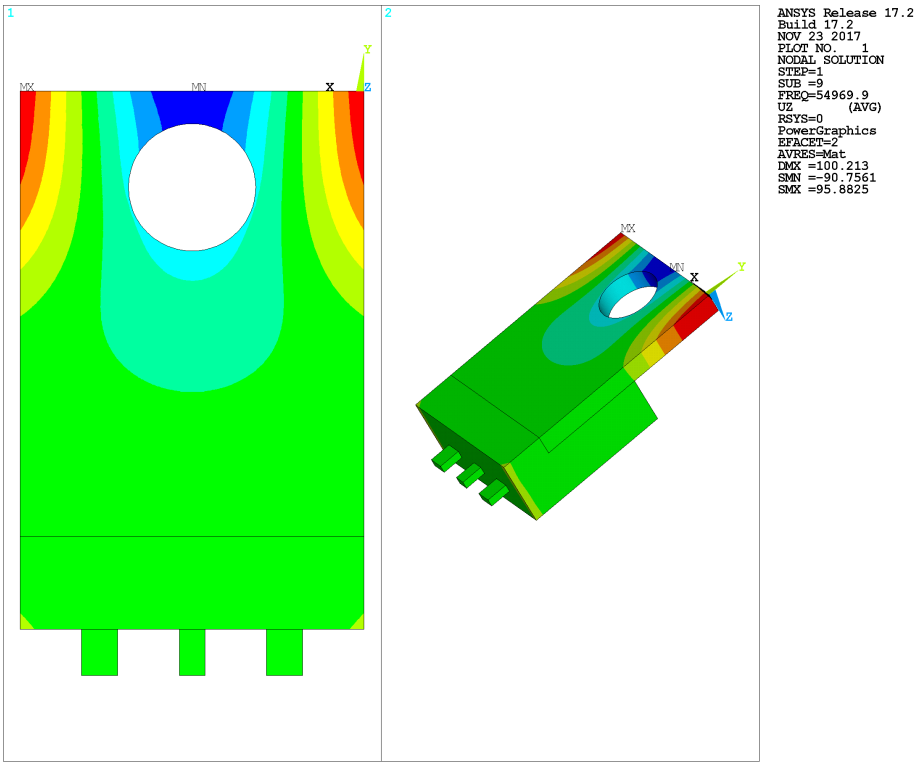


Figure 5.17: Exemplary result of the modal analysis, where the swinging form of the 10^{th} eigenmode at a frequency of 54 969.9 Hz is shown. (For the color code note that red marks the maximum positive deflection, while blue marks the minimum deflection)

Figure 5.17 shows one exemplary result of one modal solution. In this simulation the first 30 eigenmodes, with corresponding eigenfrequencies ranging from 698 Hz to 186 300 Hz, were simulated.

These simulation results need to be compared with measurement results. However, comparing the frequencies alone is not enough, since the the simulation result yields the solution of the linear i.e. the undamped model. Thus, the comparison must also ensure that the swinging forms are the same. The mathematical way for this comparison is the use of a Modal Assurance Criterion (MAC) [PBH12].

The MAC can be defined in multiple ways, depending on the exact application [All03]. Here the following definition is used:

$$MAC = \frac{|\Phi_{sim} \cdot \Phi_{mes}|}{|\Phi_{sim}| \cdot |\Phi_{mes}|}, \tag{5.9}$$

where Φ_{sim} and Φ_{mes} are the simulated and measured eigenmodes, respectively. This means that the measurement points of the eigenmodes are equally ordered into a vector. The vector of Figure 5.12 would look like

$$\Phi_{mes\ 52\,781\,\mathrm{Hz}} = \begin{pmatrix} u_1 \\ u_2 \\ \vdots \\ \vdots \\ u_{1076} \end{pmatrix} = \begin{pmatrix} 1.009\,51 \times 10^{-8} \\ 1.009\,51 \times 10^{-8} \\ \vdots \\ \vdots \\ 8.608\,53 \times 10^{-10} \end{pmatrix} \tag{5.10}$$

It can be seen in Equation (5.9) that the MAC is basically a normalised dot product of two vectors. Additionally it is known from linear Algebra that for symmetric matrices, eigenvectors to distinct eigenvalues are orthogonal to each other [Are+18]. In a modal analysis we solve the linear eigenvalue problem which can be written as symmetric matrix. This means that if one compares the simulated eigenvectors to distinct eigenvalues, one would get a MAC of zero. Comparing the eigenvectors with themselves would yield a one.

So the MAC helps in comparing the measured with the simulated eigenmodes in a mathematically correct way. To do so the vector describing the simulation must be of the same dimension as the measured one and ordered in the same way. So the same grid used in the measurements was put on the back surface of the chip in the simulation and the displacement was interpolated by the three closest nodes. Then a matrix comparing all measured with all simulated eigenmodes was calculated.

In Figure 5.18 several things can be noticed:

- From literature [OB15] it shall be noted that a MAC value over 0.8 is considered to be a match.
- A line of matches (dark dots from the lower left to the upper right) can be observed. This can be interpreted/understood in a way that all the eigenmode shapes of measurement and simulation are frequency wise ordered correctly. This is a strong indication of the overall correctness of the model.
- Each measured mode can be found in the simulated modes.

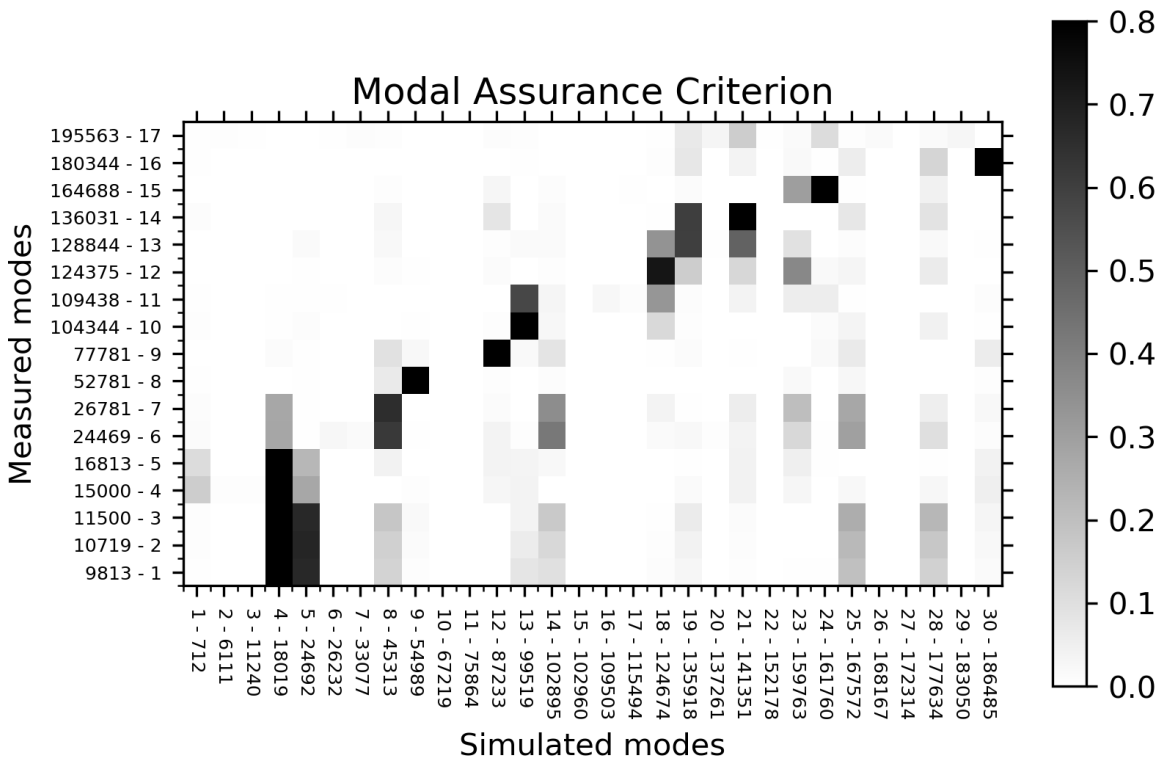


Figure 5.18: MAC matrix comparing all measured eigenmodes with all simulated eigenmodes. Note that each eigenmode is given with its mode number and its frequency.

- Not every single simulated eigenmode can be identified in the measured modes. This can be attributed to the fact that just pronounced resonance peaks in our five points (see Figure 5.10) were measured in the scan mode. If the eigenmode is hugely damped, it will not yield a pronounced resonance peak and was therefore not visible in the spectra. Since the shape of the unmeasured eigenmodes are known, it is highly unlikely that they have swinging knots in the measurement points.

- Sometimes black dots align to vertical lines. This can be further understood if we compare all measurements with each other with the MAC as in Figure 5.19. Figure 5.19 shows clusters of dots which means that some measured eigenmodes are almost equal, but were measured several times at different frequencies because they show side peaks in the spectrum.

- Simulated eigenmodes show higher frequency values than their measured counterparts. This results from the fact that a damped oscillator always has a lower resonance frequency than an undamped one [Dem18].

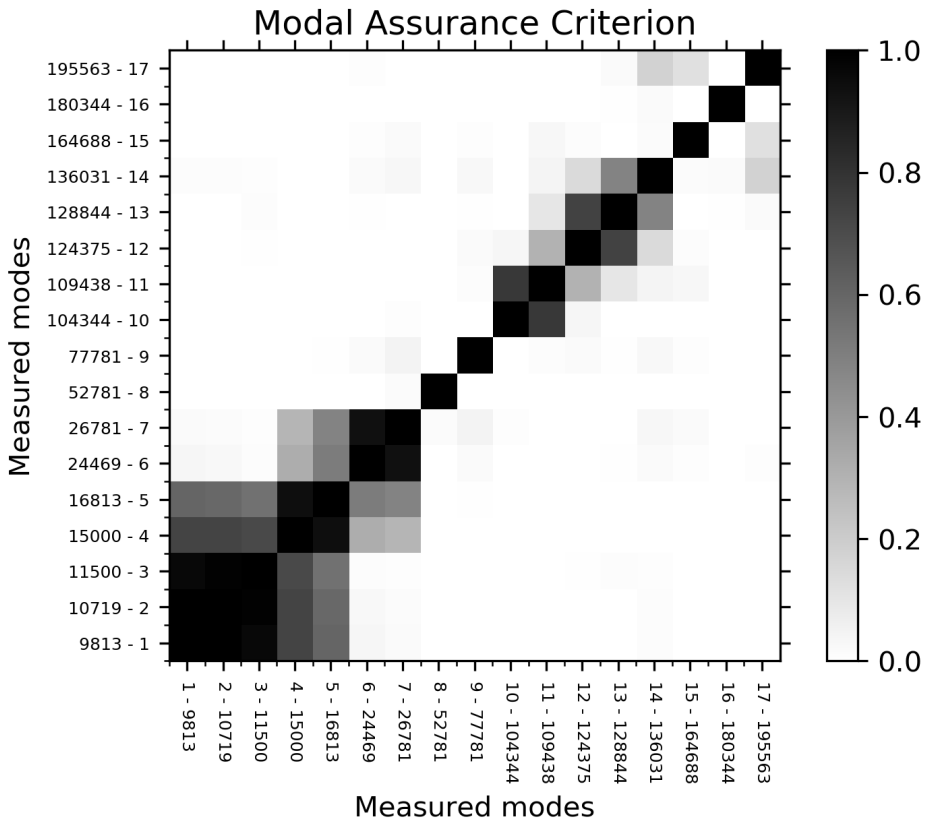


Figure 5.19: MAC matrix comparing all measured eigenmodes with each other.

Figure 5.18 shows that the main resonance measured at 52 781 Hz (compare with Figure 5.12) can be clearly identified with the simulated resonance at 54 670 Hz (compare with Figure 5.17). Since from the resonance spectra this is the one with the highest deflection, this will be the resonance we focus on. The follow up step will be a harmonic analysis of exactly that resonance.

5.6 Harmonic simulations

A harmonic analysis solves a FEM model at a certain frequency and includes all the excitation and damping effects. This means that the excitation in this model is applied by a sinusoidal voltage on the piezoelectric layer and the damping by the damping properties of the Copper and the mould compound. Due to the inclusion of the damping, the resonance frequency shifts to lower values compared to the modal analysis. This makes it necessary to simulate a broad frequency window below the undamped frequency to

identify the damped resonance. This is done in a first step by laying out a linear space frequency grid on which the harmonic solution is calculated.

The solution of each harmonic simulation on this grid is the reaction (deformation) of the system to a harmonic excitation at a specific frequency. To find the exact damped resonance frequency, a single point[3] was taken and its maximum displacement plotted against the frequency. With a fit through these points, a very accurate estimation of the damped resonance frequency can be retrieved. Around this frequency, logarithmically spaced harmonic simulations are conducted once again and the single point deformation is plotted against the frequency.

This procedure enables a very big density of simulations around the exact frequency to properly capture the resonance maximum, which is critical for comparison with the measurement. Fitting Equation (5.6) into the simulated points finally reveals the damped simulated resonance.

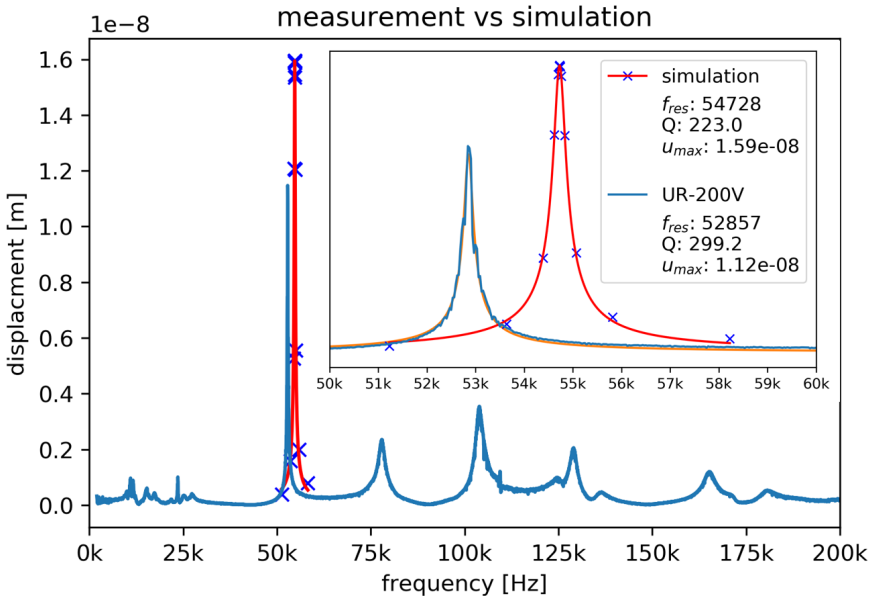


Figure 5.20: Result of the harmonic simulation. Each blue cross is the result of one single simulation. For easier visual inspection the blue crosses are fitted with the red line. The purple line is the measured deformation of the same point. (Orange depicts the fit of the measured result)

Figure 5.20 shows the result of the pre-centered logarithmically spaced harmonic simulations. With the fitted curve, the maximum and the quality factor can be easily obtained.

[3]For comparison reasons, one of the points from the spectral measurement was taken.

Comparing the measured resonance with the simulated reveals the following details that need to be pointed out:

- The modal simulation in combination with the MAC ensures that the right eigenmodes are compared with each other.
- The maximum deflection in the simulation is 13 % higher compared to the measurement. This indicates that the model is not enough damped, since larger damping would result in smaller deformation amplitudes.
- The quality factor of the simulated resonance is higher than in the measurement. This also indicates that the system is not enough damped.
- The simulated resonance frequency is higher than the measured one, which also indicates a lack of damping in the overall system.

The details above strongly indicate the lack of damping or the over excitation of the system. The next section will dive deeper into these crucial elements.

5.6.1 Excitation and damping

The excitation of the mechanical system is done via the inverse piezoelectric effect of GaN. As described above, the stack of the adaption layer and pure GaN were homogenized to get a bigger minimal feature size in the overall model. The homogenization was done following the approach of Berger et al. [Ber+05].

The used stack configuration was modeled creating a small pillar. The lateral length of the pillar was 10 µm.[4]

The boundary conditions for each material constant (C_{xx} and e_{xx}^{eff}) were applied in a way that the overall governing equation Equation (5.11) yields, zero in each line except the specific line containing the desired variable.

$$\begin{pmatrix} \bar{T}_{11} \\ \bar{T}_{22} \\ \bar{T}_{33} \\ \bar{T}_{44} \\ \bar{T}_{55} \\ \bar{T}_{66} \\ \bar{D}_1 \\ \bar{D}_2 \\ \bar{D}_3 \end{pmatrix} = \begin{pmatrix} C_{11}^{eff} & C_{12}^{eff} & C_{13}^{eff} & 0 & 0 & 0 & 0 & 0 & -e_{13}^{eff} \\ C_{12}^{eff} & C_{11}^{eff} & C_{13}^{eff} & 0 & 0 & 0 & 0 & 0 & -e_{13}^{eff} \\ C_{13}^{eff} & C_{13}^{eff} & C_{33}^{eff} & 0 & 0 & 0 & 0 & 0 & -e_{33}^{eff} \\ 0 & 0 & 0 & C_{44}^{eff} & 0 & 0 & 0 & -e_{15}^{eff} & 0 \\ 0 & 0 & 0 & 0 & C_{44}^{eff} & 0 & -e_{15}^{eff} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & C_{66}^{eff} & 0 & 0 & -e_{13}^{eff} \\ 0 & 0 & 0 & 0 & e_{15}^{eff} & 0 & \epsilon_{11}^{eff} & 0 & 0 \\ 0 & 0 & 0 & e_{15}^{eff} & 0 & 0 & 0 & \epsilon_{11}^{eff} & 0 \\ e_{13}^{eff} & e_{13}^{eff} & \epsilon_{33}^{eff} & 0 & 0 & 0 & 0 & 0 & e_{33}^{eff} \end{pmatrix} \begin{pmatrix} \bar{S}_1 \\ \bar{S}_2 \\ \bar{S}_3 \\ \bar{S}_4 \\ \bar{S}_5 \\ \bar{S}_6 \\ \bar{E}_1 \\ \bar{E}_2 \\ \bar{E}_3 \end{pmatrix} \tag{5.11}$$

Table 5.3: Mechanical and piezoelectric material parameters for the equivalent homogenized material.

material parameter	used value
C_{11}	389.38 GPa
C_{12}	144.78 GPa
C_{13}	106.17 GPa
C_{33}	397.98 GPa
C_{44}	105.21 GPa
C_{66}	122.30 GPa
e_{15}	$-0.220\,\mathrm{C/m^2}$
e_{31}	$-0.320\,\mathrm{C/m^2}$
e_{33}	$0.397\,\mathrm{C/m^2}$
ϵ_{11}	7.62
ϵ_{33}	5.30

It is important to note here that no fitting or free parameters were used in this homogenization. Of course various uncertainties arise with this homogenization. Electric polarisation interaction effects between the various single layers of the adaption layer have not been taken into account for example.

The material stack of GaN was homogenized according to this method. This artificial material (see Table 5.3 for the resulting values) was used to excite the system.

The opposing force in the model, the damping, was introduced by two materials. The Copper lead frame was given a constant damping [Smi76], whereas the damping of the mould compound was given a Prony series to model its behavior over frequency. In some more details, a Prony series Equation (5.12) is defined [Koh19] as:

$$\begin{aligned} \sigma_{mech} &= \int_0^t 2G(t-\tau)\frac{de}{d\tau}d\tau + I\int_0^t K(t-\tau)\frac{d\Delta}{d\tau}d\tau \\ G(t) &= G_0\left[\alpha_\infty^G + \sum_{1=1}^{n_G}\alpha_i^G exp(-\frac{t}{\tau_i^G})\right] \\ K(t) &= K_0\left[\alpha_\infty^K + \sum_{1=1}^{n_K}\alpha_i^K exp(-\frac{t}{\tau_i^K})\right] \end{aligned} \tag{5.12}$$

where $G(t)$ and $K(t)$ are the Prony series for shear and bulk-relaxation moduli. Rearranging the equation yields a damping over frequency plot, which is more intuitive to interpret.

[4]Bigger dimensions were used but showed no deviating results.

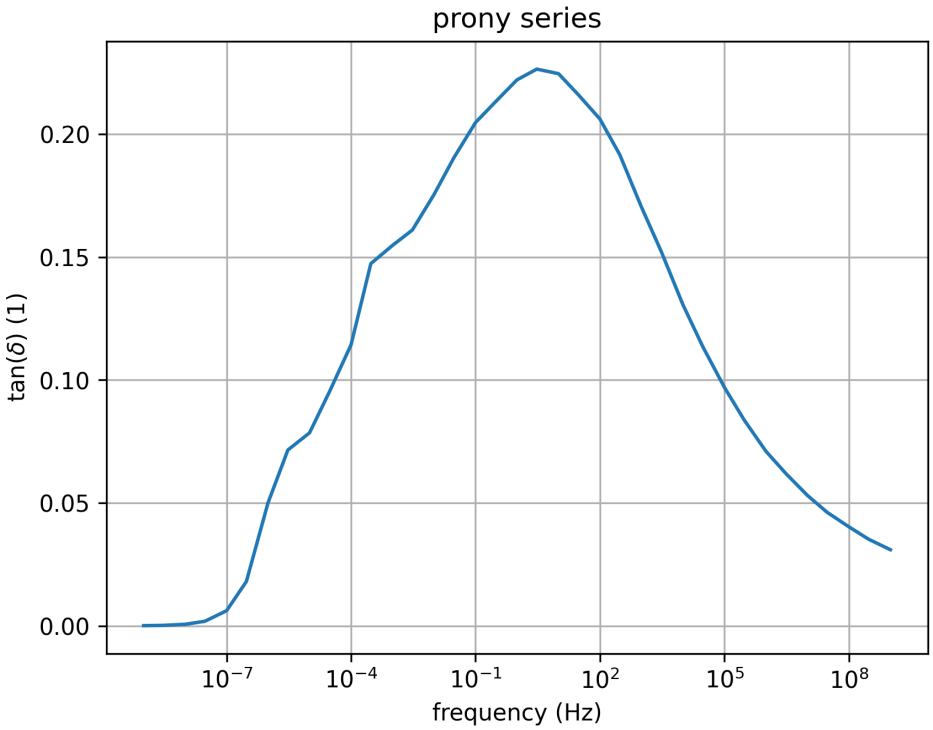


Figure 5.21: Representation of the prony series as loss modulus $\tan(\delta)$ over frequency.

The combination of the damping effects of Copper and mould compound (see Figure 5.21) plus inertia are the counteraction forces against the excitation from the homogenized GaN layer. Please keep in mind that there are no fitting parameters in all the excitation and damping factors in the model. Therefore, the mentioned 13 % difference in deflection is an excellent value!

5.6.2 Harmonic results

For the harmonic simulation the same model as for the modal analysis was used. The GaN, Copper and mold compound properties were added as described in the upper sections. The results yield an insufficient resolution in the areas of interest, namely the edges of the GaN layer and the die attach, where the peaks of the stress can be seen.

This makes it impossible to get reliable stress values and therefore a reliable assessment of the failure prone layers. In a first approach it was tried to implement a bigger element density at the border of these layers. Since a conformal mesh with no contact elements was used, this method was not able to circumvent this problem without an exploding

amount of elements in the overall model.[5] To tackle this problem a FEM method called submodeling was applied.

5.7 Submodeling

Submodeling allows to define a region of interest within a model and just simulate this region as if it was within the complete model. This makes it possible to significantly reduce the volume to model and therefore allows to increase the element density within, while keeping the number of elements in check. The boundary conditions applied at boundaries between the volume of the submodel and the complete model are called cut boundary conditions. These cut boundary conditions need to lay a bit away from the region of interest so they do not influence the results there.

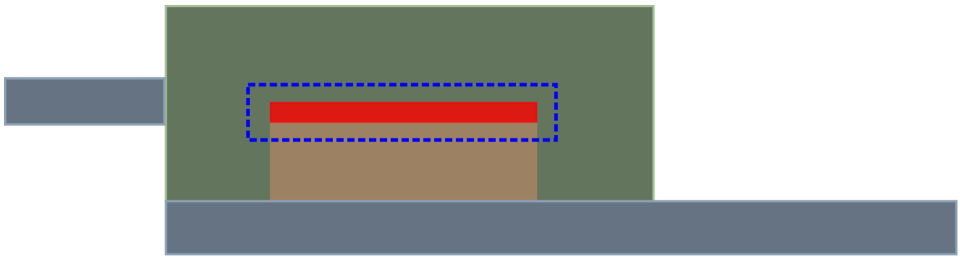


Figure 5.22: Schematics of the cut boundary conditions within the TO-220 assembly.

Exemplary, the boundary conditions for the GaN layer are depicted in Figure 5.22. This is done accordingly also for the die attach layer.

After meshing the submodel volume, the deformation at the boundary surface in the big model is applied as a boundary condition to the submodel. All forces acting within the big model need to apply also in the submodel shown in Figure 5.23.

In principle three forces act on the submodel, the deformation from the cut boundary surfaces (u), the acceleration forces (a) and the piezoelectric forces (U). However, in order to reduce computational effort, just the moment of highest stress during a swinging cycle (the point of maximum deflection in our case) is simulated in a static analysis. This neglects, both static piezo-electric and inertia forces.

[5]Note: This is due to the fact that one should no exceed certain aspect ratios in elements (ANSYS uses 1:20 as a limit). Smaller element sizes in an area therefore lead to an overall greater number of elements.

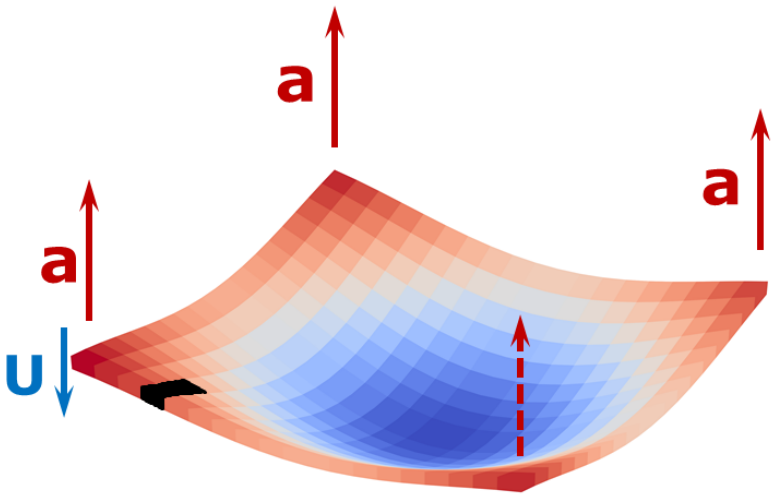


Figure 5.23: Schematics of all the forces acting on the submodel.

Table 5.4: maximum normal stress in x and y direction in the GaN layer.

	σ_x	σ_y
Full model (u, a, U)	255 kPa	255 kPa
No piezo (u, a)	260 kPa	260 kPa
No acceleration (u, U)	250 kPa	250 kPa
Bare boundary (finally used)	255 kPa	255 kPa

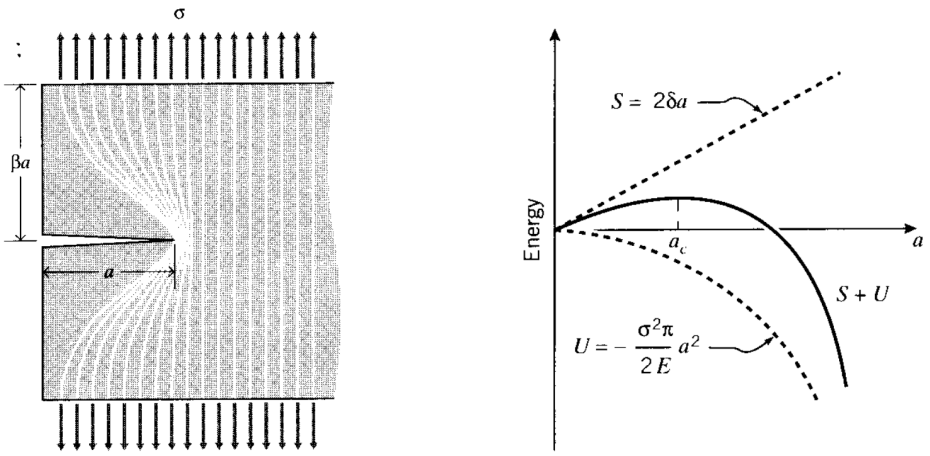
Table 5.4 shows the influence of the negligence of forces on the highest normal stress at the border of the GaN layer, our measure of merit. The effect is evaluated at the point of highest stress in y and x direction. As Table 5.4 clearly indicates, a static submodel simulation using just the deflection from the cut surfaces provides enough accuracy to asses the submodeled layer. With all these simplifications layers prone for failure are assessed.

5.8 Assessment of the failure prone layers

5.8.1 GaN layer

The modeled GaN layer is a brittle material stack. A brittle material tends to not deform plastically under stress, but rather fracture under too excessive loads. There are many

very elaborate assessment criteria for brittle materials, but for complex criteria not all coefficients for GaN are available in literature. For this purpose, a simple estimation based on Linear Elastic Fracture Mechanics (LEFM) [Roy01] [GS11] and available (mode-I) fracture toughness (K_{Ic}) values is used. LEFM in principle balances the elastic strain energy released by crack growth with the energy needed to create two new surfaces. It assumes the pre-existence of a crack of length a and a uniform stress state in the material far away from the crack, σ_∞, equivalent to the stress-state in the flaw-less material. If the stress on the crack and therefore the possible energy released is big enough, the crack will initiate as illustrated in Figure 5.24.



(a) Plate with pre-crack. The roughly triangular stress free area can be seen to both sides of the crack

(b) Energy balance between S, the energy needed to form the two new surfaces and U, the energy released by relaxing stress to both sides of the crack

Figure 5.24: Principal of the K_{Ic} fracture toughness criterion.

The stress-intensity factor K is defined as

$$K = \sigma_{mech}\sqrt{\pi a}Y \tag{5.13}$$

with the dimensionless geometry factor Y. K is related to the stress field in the vicinity of the crack tip and can directly be converted into the energy release rate G. The fracture criterion states that a crack will grow if K exceeds a critical value

$$K \geq K_c. \tag{5.14}$$

This parameter K_c is called the fracture toughness (for given crack-opening mode) and is a material parameter. A literature value for GaN in crack-opening mode I is $K_{Ic} = (0.79 \pm 0.10)\,\mathrm{MPa}\sqrt{\mathrm{m}}$ [Dro+96].

Assuming a pre-crack already introduced in production in the range of 400 µm (a larger crack would be easily spotted and the chip inked out accordingly), a maximum normal stresses can be calculated. Using a geometry factor around 2 , for crack on the edge of a plate, all values are known. Combining these values yield, a maximum stress of 10 MPa the GaN layer can withstand, which is far away from the actual stress of 200 kPa and gives a safety factor of 50 . A very unlikely '6-sigma-event' where the fracture toughness is reduced to 0.2 MPa$\sqrt{\text{m}}$, yields a maximum withstandable stress of 2.5 MPa before the crack starts to grow. This still is more than one order of magnitude away from actual stress levels. It can therefore be concluded that the mechanical resonance will not harm the GaN layer.

5.8.2 Die attach layer

In contrast to the GaN layer the die attach layer, in the case of our test chip a solder, is a ductile material. This means it can be deformed significantly plastically without fracturing and therefore needs other concepts to be evaluated. This change in behavior needs a different assessment method, since in contrast to a brittle material which exhibits a fail or pass behavior under stress, ductile materials can accumulate damage under loads which where sustained by cycles before. Such a behavior can be explained by a Wöhler curve or line, sometimes called S-N curve. (Such a curve can be seen in Figure 5.25)

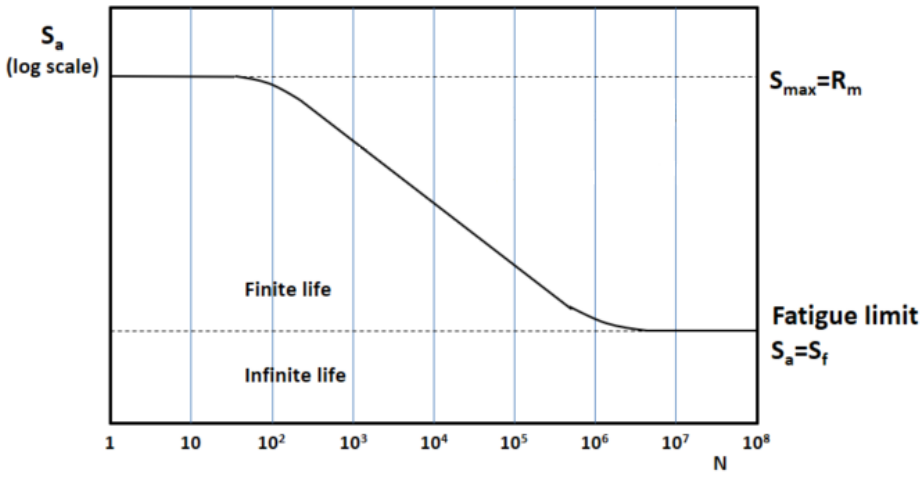


Figure 5.25: Exemplary S-N curve. [Hom18]

The exemplary S-N curve shown in Figure 5.25 shows that this material is able to withstand a certain load N times. If one increases the load this number of cycles to failure is reduced. The other way round, if the load is decreased the material can withstand

more cycles. If one follows the S-N curve to the far right, it can be observed that it gets flatter and flatter. The general interpretation is that loads will never cause a failure. This limit is known as the endurance limit of a material.

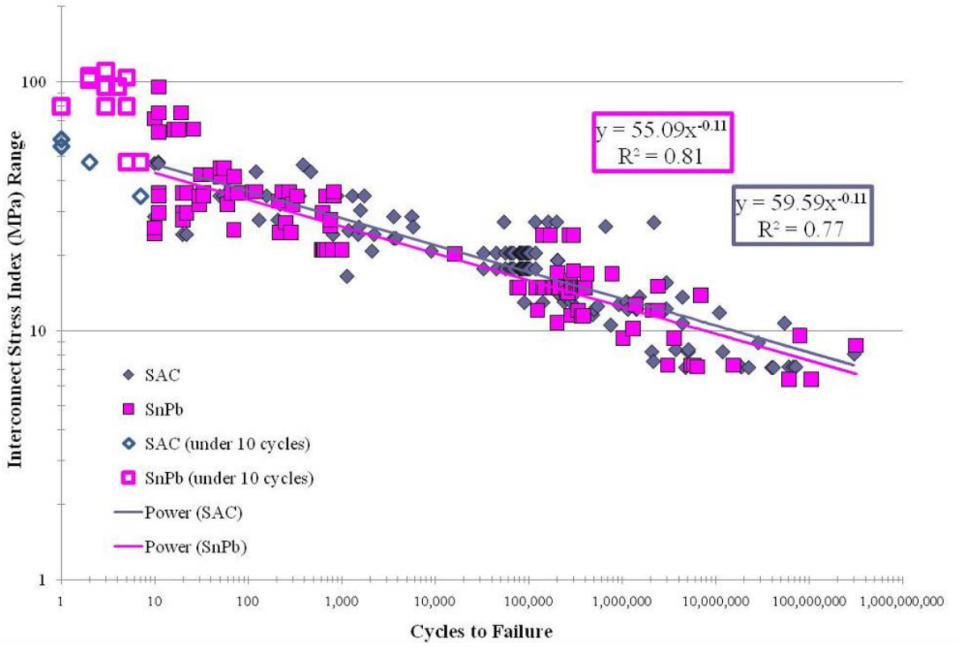


Figure 5.26: Exemplary SN curves of SnPb and SAC solder. [Paq10]

As shown in earlier sections the resonance frequency of the highest resonance is around 50 kHz. Assuming an expected lifetime of 15 yr and a duty cycle of 80 % yields $N_{cyc} = t \cdot f \cdot D \approx 2 \cdot 10^{13}$ number of cycles. This number of cycles places this problem in regime of ultra high cycle fatigue. Since no high cycle fatigue data on the specific solder used in this assembly is available following [Pri+20], data from typical solders are used. Following a very conservative approach the worst performing solder there is used. This would render the worst case in terms of solder choice. Using the magenta line from Figure 5.26 from [Paq10], inserting N yields a stress level of 2 MPa which can be withstood.

The submodel of the die attach is done in same simplified manner as the submodel of the GaN layer.

Figure 5.27 shows the von Mises stress in the die attach with its maximum of 0.2 MPa. The stress must be doubled to consider the symmetric compression and tension. This results in a safety factor of 5 , making it safe to assume that high cycle fatigue is not an issue in the mechanical resonant use case. Additionally it must be considered that the strict power law extrapolation is a rather conservative approach. It completely neglects

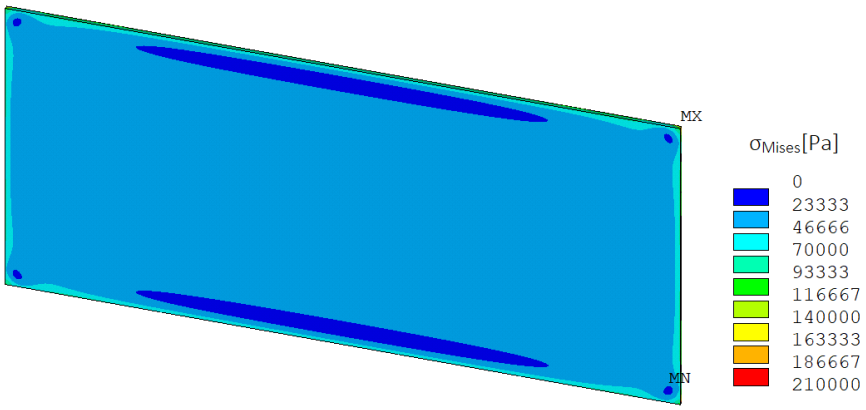


Figure 5.27: Von Mises stress of the die attach layer.

the presence of an endurance limit, which for example [Bar+07] reports around 10 MPa to 20 MPa. The actual stress levels combined with the second argument makes the resonance application of a GaN chip safe to from a a mechanical resonance point of view.

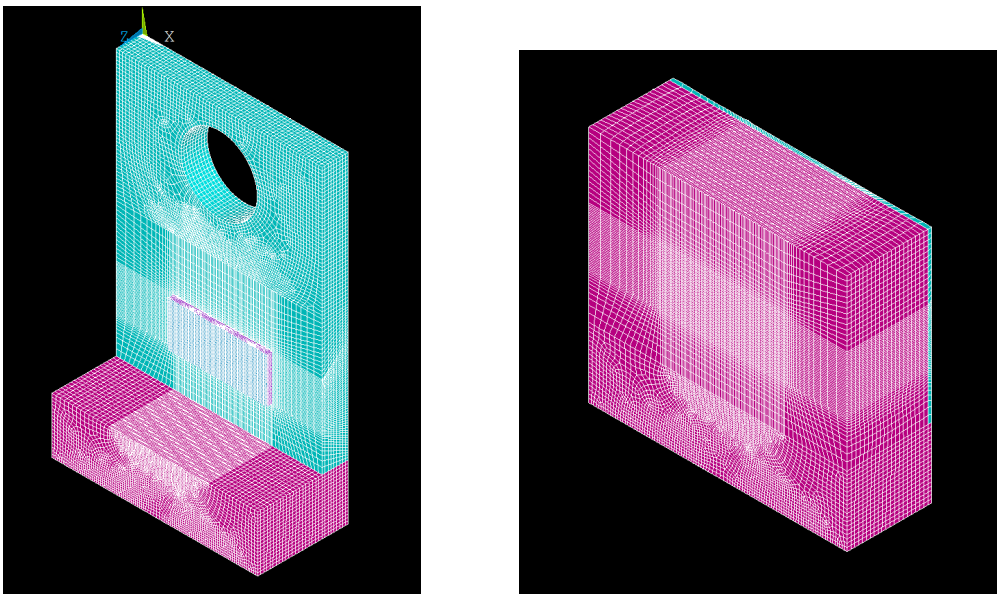
5.9 Worst case scenarios

Up to now just the TO-220 assembly of our test chip has been investigated. Since GaN technology thrives for high frequencies it is used in more modern packages, making it possible to further exploit its advantages. Therefore in this section two different extreme cases, covering most of the package trends will be investigated by modifying the TO-220 model used so far

- The first case covers a TO-220 with a greatly reduced mold compound. As can be seen in Figure 5.28 (a) the mold compound is reduced completely around the chip itself.

- The other case will cover the case with a greatly reduced lead frame. The lead frame is there thinned down to 200 µm.

Modifying in one case the mold compound and in the other the lead frame gives greater insights on how the overall system reacts to changes in the principle damping materials. To both cases the same work flow (without the comparison to the experiment, due to the lack of samples) has been performed.



(a) Extreme case with extremely reduced mold compound

(b) Extreme case with extremely reduced lead frame

Figure 5.28: Schematics of the extreme cases.

Since the mechanical body is significantly altered in both cases also the frequency spectrum is different. For both models the same eigenmode as in the complete TO-220 model is assessed to be able to compare the cases.

For the thinned lead frame case the stresses in the solder increase by about 20 % to 0.25 MPa. Again multiplying by 2 , the safety factor is still about 4 . In contrast the extreme case of heavily reduced mold compound the stresses in the solder, increase significantly to 2.3 MPa This stress level is already over the limit extrapolating the S-N curve. Nevertheless, literature indicates that the endurance limit is in the range of 10 MPa to 20 MPa and therefore still a factor of 4 away from the extreme case stress levels in the solder.

Looking at the stress levels in the GaN layer in the case of the reduced lead frame yield an increased maximum stress of 350 kPa which is still far away from the limit to further open a crack. The realization with the bare minimum of mold compound shows higher stress level from about 1 MPa still at least a factor 10 away from the critical limit.

Therefore also in this hypothetical case of a “bare die mounted on Copper” no true reliability risk should be expected, we suggest that for power-GaN assemblies with minimum mechanical damping, special attention should be paid to potential ultra-high cycle fatigue damage in the die attach by mechanical resonance effects.

Chapter 6

Conclusion

6.1 Summary

In this thesis two, to power electronics semiconductor new phenomena that are not present in conventional Silicon (Si) devices were investigated and explained. Furthermore, the principle interaction of mechanical stress, temperature and potential was shown.

The first effect under investigation was massive thermal overload produced by a short circuit until end of life. In contrast to common Si devices, which suffer from thermal runaway above certain temperatures and are thus limited in robustness in short circuit, Gallium Nitride (GaN) High Electron Mobility Transistors (HEMTs) suffer from a different failure mode. As shown in Chapter 4, GaN devices in short circuit fail into a permanent off state, caused by a protrusion between gate and source. From an electrical point of view this fail to off state is the preferred behavior. The root cause of this behavior was identified by means of advanced physical failure analysis combined with thermo mechanical simulations. Due to the small power dissipation area in the two-dimensional electron gas (2DEG), temperatures in and around the gate finger rise very quickly. This temperature rise in combination with the different Coefficients of Thermal Expansion (CTEs) of the gate finger aluminium and the surrounding imide leads to a protrusion between gate and source. With simulation, the point of maximal stress could be identified and matched with the location on the analyzed chips. Improvements from a design point of view were discussed with the conclusion that the geometry features already in use are very close to optimal. Further improvements are just possible by changing the gate finger metal, which heavily influences the design in general.

The second phenomenon discussed arises from the fact that GaN is a polar material making it piezoelectric. The reverse piezoelectric effect, converting voltage to deformation,

results in resonance phenomena in the chip. These resonances and their implications on lifetime were investigated in Chapter 5. Since measurements of mechanical stress within the chip while undergoing a resonance are very difficult to perform, a simulation approach was chosen. For simplification of the simulation, the physical tests were performed on a test chip, which only features a vertical field. The result from the measurements on the test chip were used to calibrate the mechanical simulation. This was done by a two step process, first comparing the deformation shapes by a mathematical concept called Modal Assurance Criterion (MAC) and then investigating a single resonance in depth by the size of the deflection. This made it possible to validate the simulation of the test chip. Following that, the simulation allowed for in depth investigations of the identified critical layers, namely the GaN and the die attach layer. The brittle GaN layer was assesed by means of the crack model of K_{1c} yielding no risk for cracking. Secondly the ductile die attach solder was investigated by ultra high cycle fatigue Wöhler curves also showing no signs of reliability issues. To complete investigations extreme cases of ultra thin lead frames and heavily reduced mold compound realizations of the chip were assessed. These cases also showed no significant reliability implications.

6.2 Outlook

The new material system GaN and the new device type HEMT still have a long way to go to reach similar levels of understanding as they are already present in Si. From the basic concept of a GaN HEMT it is necessary to go to new packaging concepts reducing parasitic effects further to fully exploit the natural capabilities of GaN. These packages will become smaller and smaller offering less damping compared to the test device investigated in this thesis. Further studies for these very advanced package designs might be necessary in the future. The modeling framework used in this thesis can be used as a starting point for this even though the additional challenges need to be overcome. The most prominent one will be capturing the stiff connection of soldered Surface-Mount Device (SMD) devices on printed circuit board (PCB), which will make it necessary to model the whole assembly or large portions of it. This work is left for the next generation of researchers further increasing our knowledge on GaN.

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List of Figures

Acronyms

2DEG two-dimensional electron gas

AlGaN Aluminium Gallium Nitride

AlN Aluminium Nitride

APDL Ansys Parametric Design Language

BKIN Bilinear Kinematic Hardening Plasticity

CAD Computer-Aided Design

CTE Coefficients of Thermal Expansion

DAC Digital-to-Analog Converter

DoF Degrees of Freedom

DUT Device Under Test

FE Finite Element

FEA Finite Element Analysis

FEM Finite Element Method

FIB Focused Ion Beam

GaN Gallium Nitride

HAADF High-Angle Annular Dark-Field

HEMT High Electron Mobility Transistor

HV High Voltage

ILD Inter-Level Dieelectric

LEFM Linear Elastic Fracture Mechanics

LSDV Laser Scanning Doppler Vibrometer

MAC Modal Assurance Criterion

MOSFET Metal-Oxide Semiconductor Field EffectTransistor

NBTI Negative Bias Temperature Instability

PBTI Positive Bias Temperature Instability

PCB printed circuit board

PDE Partial Differential Equation

PEM Photo Emission Microscopy

PFC Power Factor Correction

SEM Scanning Electron Microscopy

Si Silicon

SiC Silicon Carbide

SMD Surface-Mount Device

SOA Safe Operating Area

STEM Scanning Transmission Electron Microscopy

TCAD Technology Computer-Aided Design

TEM Transmission Electron Microscopy

List of Symbols

A cross section area

A_{cap} area of a plate capacitor

A_{ind} cross section area of the inductor

C heat capacity

C_{xx} elasticity matrix

E electric field

E_{mech} Youngs modulus

I second moment of area

I_D drain current

K stress intensity factor

L inductance

P polarisation

Q_{dev} power dissipation of the device

Q_{mech} mechanical quality factor

$R_{ds,on}$ on resistance of a device between drain and source

T temperature

T_J junction temperature

T_x ground temperature of the system

U voltage

V_{DS} drain source voltage

V_{GS} gate source voltage

V_{th} threshold voltage

W_{el} electric field energy

X_L impendance of a inductor

Y geometry correction factor

α angel between the moving object and the laser

α_c coefficient of thermal expansion

α_{therm} thermal diffusivity

$\boldsymbol{D}$ electric displacement

$\boldsymbol{S}$ strain vector

$\boldsymbol{T}$ stress vector

ϵ_0 vacuum permittivity

ϵ_r specific permittivity

ϵ_{mech} mechanical strain

λ wavelength

ν poisson ratio

ρ volumetric mass density

σ_q charge area density

σ_{mech} mechancial stress

τ characteristic time of the temperature build

θ_{Jx} steady state thermal resistance of the system

b width

d_q distance between charges

d_{cap} distance between the plates of a plate capacitor

d_{piezo} piezoelectric coefficient matrix (stress form)

e_{xx}^{eff} piezoelectric coefficient matrix (strain form)

f_b frequency shift from the Bragg cell

f_d frequency shift

h height

k thermal conductivity

k_x wave vector

l length

m arbitrary scaling factor

p electric dipole moment

p_{pyro} pyroelectric coefficient

q heat flux

q charge

r_{ind} radius of the inductor core

s compliance matrix

v velocity

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